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Epitaxial Oxide Devices: Fabrication and Characterization at the Nanoscale

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Abstract

Oxide Spintronics is an emerging research direction in Spintronics today. The exceptional electron charge/orbit/spin correlation present in these complex oxide thin films has produced several fascinating physical phenomena. In this work, half metallic oxides as $La_{0.67}Sr_{0.33}MnO_3$, believed to have 100% spin polarized carriers have been used to fabricate epitaxial diodes which are the building blocks of any electronic devices. Very little is known about the interface between typical half metallic ferromagnets and non-conventional semiconductors as doped $SrTiO_3$. The epitaxial interface formed in such systems coupled to the half-metallicity can give rise to interesting insights into the physics of these complex oxides. In this thesis, the versatile technique of Ballistic Electron Emission Microscope has been used to study the local electron transmission as a function of energy across an epitaxial interface between $La_{0.67}Sr_{0.33}MnO_3$ and Nb doped $SrTiO_3$. Such a study, done for the first time, reveals interesting features in the local transmission, which can be correlated with the electronic and structural properties of these materials and the underlying substrate at the nanoscale.

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Chapter 1: Introduction

The burgeoning field of Spintronics relies heavily on new materials that show interesting magnetic properties. Gaining a deeper understanding of different ferromagnetic materials, and in particular their spin dynamics, is an important issue in today's quickly evolving science. Although, the birth of Spintronics can be traced back to late 80s when the giant magneto resistance effect was first observed in magnetic multilayer systems, a great amount of work has been done, since then, leading to further developments in the field. Oxide Spintronics is one such emerging research direction and holds rich promise specially, in the realization of an all-oxide electronics.

1.1. Spintronics

The very fundamentals of Spintronics are based on the spin of electrons. The spin of an electron is a fundamental property that originates from an electron's spin around its axis. Depending on the direction of the angular momentum that this spinning causes, electrons can have spin-up (when the angular momentum is pointed upward) or spin-down (when it is pointed downward). In a normal metal the number of spin-up and spin-down states and correspondingly the number of spin-up and spin-down electrons are the same. However, in a ferromagnet, the number of one of the spin-states, as it is shown in Figure 1.1, is more than the other spin states (called the minority spin-states), causing the material to have a net magnetization direction while resting in its Fermi energy level.

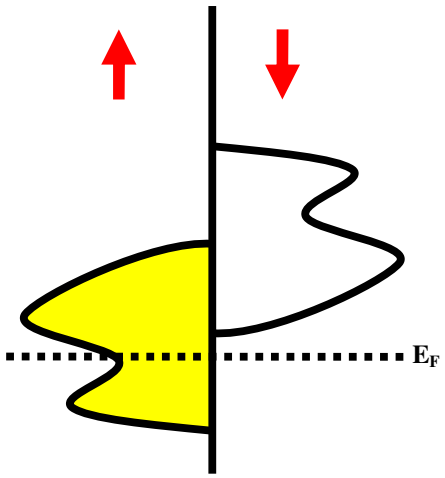

Figure 1.1 Spin-up and spin-down states around Fermi level. Only spin-up states are occupied by the electrons at Fermi energy.

Giant Magneto-Resistance (GMR) technology uses this spin property of electrons to detect a high or low current signal that later is respectively interpreted into one or zero digits to be used in data processing units. A simple GMR stack consists of a non-ferromagnetic layer sandwiched between two ferromagnetic layers. If the direction of

magnetization in two ferromagnetic layers is aligned in the same (opposite) direction the traversing electrons encounter the minimum (maximum) scattering from the second ferromagnet after being polarized by the first ferromagnet, which is measurable as a low (high) voltage drop between two ferromagnetic electrodes. The first spacers, which were used as separators of top and bottom ferromagnetic layers, were conducting in nature, however, shortly after that, thin insulating spacers were proposed. Utilizing this mechanism has led to the so called Tunneling Magneto-Resistance (TMR) effect. TMR yields nearly one order of magnitude larger magneto resistance values at room temperature with respect to GMR [1] and therefore it is a good choice in making room temperature electronic devices.
TMR (or its equivalent GMR) ratio is a measure that is used to show the effectiveness of Magnetic Tunnel Junctions (MTJ). This ratio is defined as:

$$TMR = \frac{R_{AP} - R_P}{R_P} \tag{1.1}$$

Here R_{AP} (R_P) is the resistance of the ferromagnetic multilayer when the magnetization directions of the ferromagnets are anti-parallel (parallel). If spin polarization in a ferromagnetic layer is defined as:

$$P = \frac{N_\uparrow - N_\downarrow}{N_\uparrow + N_\downarrow} \tag{1.2}$$

In which N↑ (N↓) is the number of density of states at Fermi energy for spin-up (spin-down) electrons, using the TMR ratio one can show:

$$TMR = \frac{P_1 P_2}{1 - P_1 P_2} \tag{1.3}$$

This relation, called Julliere equation, is of great significance since it relates the TMR ratio to the spin polarization of the two ferromagnetic layers. In this relation P_1 and P_2 show the polarization of top and bottom ferromagnetic layers.
Figure 1.2 (a) shows the configuration by which we can see the GMR or TMR effect if the spacer between two ferromagnets is a metal or an insulator, respectively. Here the current is flowing in y-direction through the device in which the spacer is sandwiched between two ferromagnetic layers. First ferromagnetic layer polarizes the electrons that are injected into the spacer. If the magnetization of second ferromagnetic layer is parallel to that of the polarizer, electrons encounter minimum scattering from the interfaces while they are traveling through the stack. On the other hand, if the magnetization of second ferromagnetic layer is directed opposite to that of polarizer, electrons face a greater spin-dependent scattering. Considering the fact that this device can show a large or small resistance for anti-parallel or parallel orientations of the magnetizations of ferromagnets, respectively, it can work as a valve and that is why this device is sometimes called Spin Valve.

Figure 1.2 (b) shows two different magneto resistance states (i.e., when the magnetization directions of ferromagnetic layers are in parallel or anti-parallel) in a simplified way. A large TMR ratio (which corresponds to a large difference between maxima and minima in Figure 1.2 (b) is vital for better detection of spin-polarized current.

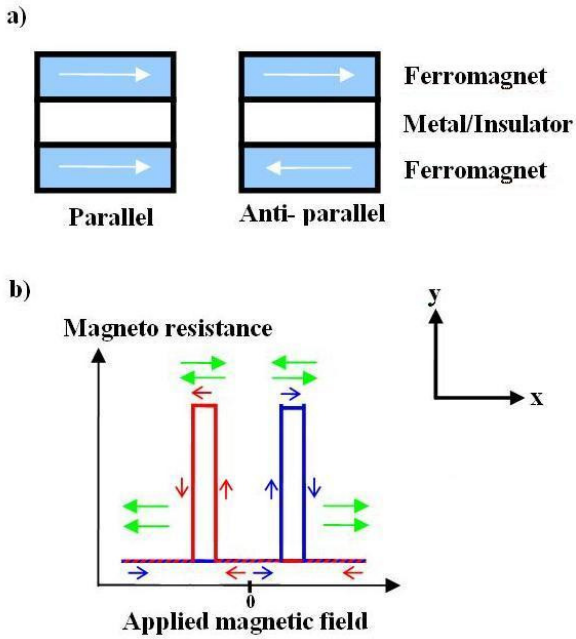

Figure 1.2 a) Device configuration of either GMR or TMR if the current is traversed in y-direction while the spacer is a metal or an insulator, respectively. b) A simplified picture of the TMR ratio versus external magnetic field.

In both GMR and TMR configurations, one ferromagnetic layer is usually chosen so that it is softer than the other, and thus can more easily change its magnetization state when an external magnetic field is applied. This is done either by choosing different ferromagnets or through shape anisotropy [2]. This allows us to control magnetization directions of different ferromagnetic layers with the applied magnetic field. Figure 1.2 (b) shows a simplified representation of dependence of the magneto-resistance on external applied magnetic field. In the left-hand side of this figure, the magnetization directions of both ferromagnets are pointed to the left and therefore the resistance of the device shows a minimum. We follow the blue arrows by decreasing the magnetic field down to zero, then switch the direction of the applied magnetic field and increase it until we change the magnetization direction of one of the ferromagnetic layers. At this moment, we see a huge resistance in the device. By further increasing the external magnetic field we change the magnetization direction of the other ferromagnetic layer and we again see a small resistance in the device. We can repeat the same kind of experiment by following the red arrows from the far right in Figure 1.2 (b), i.e. by reducing and then reversing the direction of applied magnetic field. Doing this, we would get a mirror-like image of what we got in previous case.

1.2. Oxide Spintronics

Concomitant with the development of metal-based or semiconductor-based Spintronics since the late 1980s, important advances have been made regarding ferromagnetic oxide thin films and their applications in Spintronics. The first notable record of using magnetic oxides as electrodes in magnetic tunnel junctions yielded tunnel magneto-resistances ratios that were one order of magnitude [3] larger than what had been obtained from transition-metal electrodes. Later it was found that some of ferromagnetic oxides can act as half metals (i.e. a material that only has one of spin-up or spin-down electron states in its Fermi level and therefore has a conductive nature for electrons having the spins of available states and insulating nature for the electrons having the other spin orientation. Figure 1.1 shows the spin band diagram of such a material). It is indeed very straightforward from the Julliere formula that materials having high values of spin polarization would yield high TMR ratios.

1.3. $La_{2/3}Sr_{1/3}MnO_3$

One of the remarkable impacts on the ferromagnetic oxide Spintronics came with the prediction of nearly 100% spin polarization (half metallic) in $La_{2/3}A_{1/3}MnO_3$ (with A be Ca, Sr, or Ba) [4]. Notable evidences following this theoretical prediction came with the direct experimental demonstration of half metallic nature of $La_{2/3}Sr_{1/3}MnO_3$ (LSMO) [5]. Further boosting this idea was the 1800% TMR-ratio demonstration of $La_{2/3}Sr_{1/3}MnO_3/SrTiO_3/La_{2/3}Sr_{1/3}MnO_3$ MTJ at 4 K [6]. From this TMR value a spin polarization of at least 95% is inferred, which strongly underscores the half-metallic nature of LSMO.

Figure 1.3 shows phase diagram of the $La_{1-x}Sr_xMnO_3$. In this diagram AFM, PM, PI, FM, FI and CI denote anti-ferromagnetic metal, paramagnetic metal, paramagnetic insulator, ferromagnetic metal, ferromagnetic insulator, and spin canted insulator states. We can see that the Curie temperature, T_c, at which a phase transition from ferromagnetic metal to paramagnetic metal happens, is maximum (~369 K) when x= 1/3.

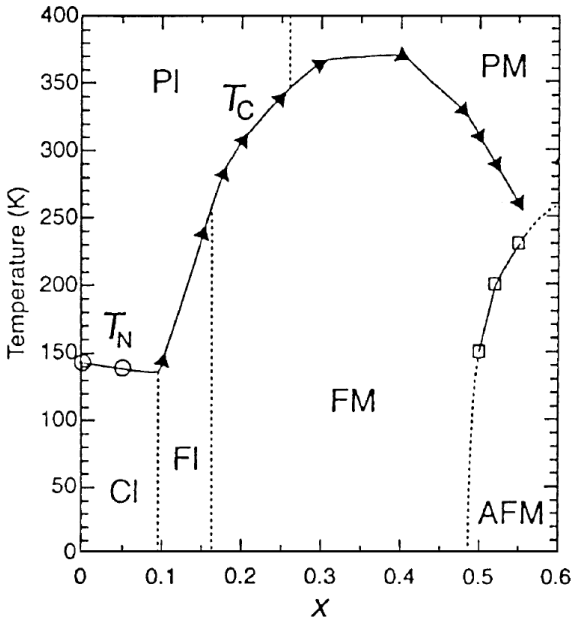

Figure 1.3 $La_{1-x}Sr_xMnO_3$ Phase diagram. AFM, PM, PI, FM, FI and CI denote anti-ferromagnetic metal, paramagnetic metal, paramagnetic insulator, ferromagnetic metal ferromagnetic insulator and spin canted insulator states, respectively [7].

Detailed experimental results suggest that LSMO does have minority spin states at its Fermi level but since its current spin polarization is much higher than that of the density of states [8], this material can mimic the behavior of a true half-metal in transport experiments.

1.4. $SrTi_{1-x}Nb_xO_3$ Substrate

$SrTiO_3$ (STO) is the best substrate choice for growing LSMO thin films. The most important reason to choose STO as the substrate is that it has a very good lattice match ($\alpha_{STO} = 0.3906\,nm$) to that of the LSMO lattice ($\alpha_{LSMO} = 0.3873\,nm$). Furthermore, STO has a thermal expansion coefficient (~11×10^{-6} K^{-1}) that is very close to that of LSMO's (~11.5×10^{-6} K^{-1} for $La_{2/3}Sr_{1/3}MnO_3$) which guarantees a crystal misfit of less than 1% for all temperatures below 1000 K [9]. STO is very well known for its high dielectric constant; at room temperature its dielectric constant is nearly 300, while it goes as high as 20000 at very low temperatures.

To perform electrical studies on the interfaces related with the STO substrates, the latter are doped with niobium. Niobium atoms sit in Titanium sites; $SrTi_{1-X}Nb_XO_3$ (Nb:STO). The amount of doping is usually referred to as weight percent of doping. In the market, various doping concentrations of the substrate are available, e.g. X = 0.01, 0.05, 0.1, etc.

1.5. Motivation

The major aim of this thesis was to fabricate epitaxial diodes of half-metals as LSMO on Nb doped STO and to characterize them. The utility of such a study is that it forms the building block on which an all-oxide epitaxial spintronics device (e.g. an oxide MTJ) can be fabricated. Further, it is now becoming increasingly clear that the interfaces in such complex material systems can lead to fascinating electronic properties [10]. However, it

is extremely challenging to probe them at the nanoscale and to obtain quantitative information of the electron transport and scattering mechanism in such systems. Ballistic Electron Emission Microscope (BEEM) is a useful technique to probe buried layers and interfaces with a high spatial resolution and at the nanoscale. Thus a major challenge of this project is to fabricate reliable and reproducible epitaxial oxide diodes and to probe the electrical transport properties of these diodes at the nanoscale using BEEM. Since no prior studies have been done in this direction in the present group or elsewhere in the world, all the parameters and protocols needed to realize such a diode had to be optimized. The thesis is divided as follows:

Chapter 2 provides a general understanding of the BEEM system and its theoretical background that helps in interpreting the BEEM data. In Chapter 3 the different experimental techniques, which have been used in our device characterization, are briefly discussed. Chapter 4 deals with the results of the electrical characterization of the oxide substrates. In this chapter, the results of resistivity, carrier concentration, and mobility are presented for the substrates, that were used in this work. In Chapter 5, all steps required in the realization of a LSMO/NbSTO diode are presented as well as the results of our studies on LSMO-film characterization. We conclude this chapter by providing the results of two-probe transport studies on the fabricated diodes. The results of the first BEEM studies done on such epitaxial systems are presented in Chapter 6, which also discusses the origin of the intriguing electron transmission characteristics, at the nanoscale, in such epitaxial LSMO/NbSTO systems. At the end, a summary of all the discussions in this thesis is presented in Chapter 7.

Chapter 2: Ballistic Electron Emission Microscopy

Complete fundamental understanding of metal-semiconductor(MS) interfaces is not possible by conventional Schottky barrier characterization methods (e.g. current-voltage(I-V) or capacitance-voltage(C-V) measurements). Since they are limited by their lack of spatial resolution while probing the M-S interface, it is only possible to get the macroscopic overview of the diode. On the other hand, Ballistic Electron-Emission Microscope (BEEM) has been shown to be a powerful nondestructive technique which can directly probe the local Schottky barrier interfaces with high spatial resolution. It is also possible to get a nanometer scale direct visualization of the M-S heterostructures by using the highly resolved imaging capabilities of such technique.

2.1. Ballistic Electron Emission Microscope

Ballistic Electron Emission Microscope (BEEM) is a three terminal modification of a Scanning Tunneling Microscope (STM). In BEEM, a STM tip (emitter) is used to inject hot electrons (energy few eV above the Fermi level) across a vacuum tunneling gap into a thin metal (base) layer that forms a Schottky contact on a semiconducting (collector) substrate. A schematic representation of the BEEM setup developed by Bell and Kaiser in 1988 [11], is shown in Figure 2.1. A fraction of the injected hot electrons after transmission in the metal base reach the metal/semiconductor interface and, if they have the necessary energy and proper momentum, these can overcome the Schottky Barrier (SB) at that interface and will be collected at the rear contact of the semiconducting substrate. In the imaging mode of the BEEM, the tip bias and tunneling current are kept fixed. The topography of the top surface is recorded while simultaneously mapping the current in the same area, commonly referred to as the BEEM image.

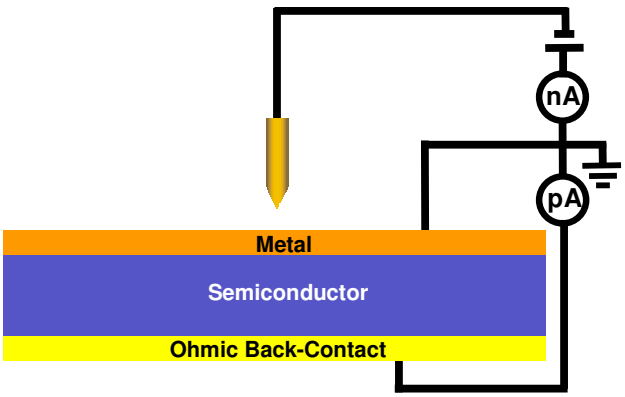

Figure 2.1 This is the schematic representation of a BEEM system. Note that there is no bias applied between the base and collector which provides the MS interface is at zero bias during the BEEM measurements.

STM study of conventional semiconductors involves tunneling between the tip and the conducting surface. In contrast, in BEEM the injected carriers are filtered at the Metal-Semiconductor (MS) interface and only the electrons having proper energy and momentum to overcome the SB height (SBH) will be collected by the contact at the rear of the semiconducting substrate. By simply varying the tip potential, the energy and angular distribution of hot electrons can be independently controlled. Further, the spatial resolution of the BEEM is quite high (~ 1.5 Å). Thus, BEEM provides, in addition to the information about the surface morphology, a combination of electron microscopy and spectroscopy with high-spatial and high-energy resolution.
It is worth mentioning that there is a critical angle for the acceptance of the propagated electrons at the MS interface, typical values varying between 2-10°. The electrons reaching the MS interface outside this cone, at that particular energy, cannot be collected. This critical angle, depends on the incident energy, momentum and interface band structure and is the dominant effect governing the transmission into the semiconducting substrate. Any scattering in the metal film reduces the number of electrons collected. Thus for a complete epitaxial system, the transmission is expected to be larger as compared to polycrystalline systems due to reduction in the momentum scattering arising due to elastic scattering events. For a complete description of BEEM, the reader is referred to [12].

2.2. Sample Requirement

One of the advantages of the BEEM is in its ability to measure signals as low as 0.1 pA. To measure such small signals, the noise level in the electronics of the BEEM system plus the noise level generated in the sample must be very low.
At finite temperatures, any resistor has voltage fluctuations across its ends, which is known as Johnson noise. The Johnson noise is given via the following equation:

$$V_{RMS} = \sqrt{4 k_B T B R} \qquad 2.1$$

In this equation, V_{RMS} is root mean square of the voltage fluctuations, k_B is the Boltzman's constant, T is the measurement temperature, B is the measurement bandwidth, and R is the value of the resistor.
For the BEEM part, the feedback resistors of STM and BEEM are the main sources of the electronic noise. A choice of low noise and proper bandwidth amplifiers can help reducing this noise. Nevertheless, to reduce the overall noise to signal ratio in the measurements, the level of noise from the sample must be kept low. Therefore, here we elaborate on sample requirements needed for an efficient measurement.
In thermionic emission theory, the current passing through a Schottky junction is given as [13]:

$$I_{Diode} = A A^{**} T^2 \, exp\left(\frac{q\Phi_B}{k_B T}\right)\left[exp\left(\frac{qV}{nk_B T}\right) - 1\right] \qquad 2.2$$

In which, A is the area of the junction, A^{**} is the modified Richardson constant (specific to the heterojunction), V is the applied voltage to the interface, Φ_B is the SBH, n is the ideality factor, and T is the measurement temperature. From this equation, the junction resistance at zero bias can be derived as [13]:

$$R_{Diode} = \left(\frac{dI}{dV}\right)^{-1}_{V=0} = \frac{k_B}{q\,A\,A^{**}\,T} exp\left(\frac{q\,\Phi_B}{k_B T}\right) \qquad 2.3$$

From equation 2.3, it is very straightforward to understand that the resistance of the MS interface can be increased either by reducing the junction area or by cooling it down to low temperature. It is worth mentioning that although at finite temperatures, the voltage across the junction starts to fluctuate, this does not affect the BEEM-current measurements. The reason being that the operational amplifier for BEEM does not measure the voltage drop across the junction, but measures the current passing through it. Based on this, the noise measured by the operational amplifier at zero bias resistance of the Schottky diode is given as:

$$I_{RMS} = \frac{\sqrt{4\,k_B\,T\,B}}{\sqrt{R_{Diode}}} \qquad 2.4$$

The above equation shows that the contribution of the sample noise to the overall noise level of the electronic system will decrease by increasing the diode's resistance, R_{Diode}.

2.3. Bell-Kaiser Model

In BEEM measurements, the tip is positioned close to the top surface of the sample under investigation. Electrons are injected via tunneling through a vacuum barrier. These electrons usually have an attenuation length of about 10 nm (different for different metals) before they ballistically reach the interface. BEEM technique provides a direct probe of the interface by measuring the collected current, I_c for different tip bias, V. Current flow from the back contact can be best described by the following equation [11]:

$$I_c = R\,I_t \frac{\int_{E_{min}}^{\infty} D(E_x) \int_0^{E_{max}} f(E)\,dE_t\,dE_x}{\int_0^{\infty} D(E_x) \int_0^{\infty} [f(E) - f(E+eV)]\,dE_t\,dE_x} \qquad 2.5$$

Where I_t is the tunneling current, $D(E_x)$ is the transmission probability for an electron to tunnel through the vacuum barrier, f(E) is the Fermi function, m_t is the electron's effective mass parallel to the interface within the semiconductor, m is free electron's mass, and R is the measure of attenuation due to scattering in the base metal layer. The terms E_{max} and E_{min} in this equation are [11]:

$$E_{max} = \frac{m_t}{m - m_t}(E_x - E_f + e(V - V_b))$$ 2.6

And,

$$E_{min} = E_f - e(V - V_b)$$ 2.7

The scattering attenuation, R, is taken to be an energy-independent constant, since ballistic attenuation length in metals is nearly independent of energy $E\text{-}E_f$ of less than 2eV. By adjusting V_b and R, equation 2.5 can be fitted to experimental data. For parabolic conduction band minimum and parallel momentum conservation at interface the I_C –V dependence becomes:

$$I_c \sim (V - V_b)^2$$ 2.8

This is valid for voltages slightly above the threshold value V_b, of the MS interface. Equation 2.8 represents the Bell-Kaiser (BK) model to explain the BEEM transmission in the MS interface [11].

2.4. Metal Spintronics

The versatile technique of BEEM has been established as an efficient mechanism to determine the SBH at local regions of a metal/semiconductor interface. When an external magnetic field is applied, spin dependent transport in magnetic heterostructures can be studied in a current-perpendicular-to-plane configuration. This technique relying of the spin dependence of electrons/holes in spin valve structures is known as the Ballistic Electron Magnetic Microscopy (BEMM). Figure 2.2 shows a BEMM study on such a magnetic spin valve. In this experiment [14], the spin dependent transmission of a n-Si/Au/$Ni_{81}Fe_{19}$(2.5 nm)/Au/Fe(1 nm)/Au spin valve, in the parallel and anti-parallel configuration of the two magnetic layers are shown. In part (a) of this figure, we see that the BEMM current versus tip bias has different values for the parallel and anti-parallel configurations of the two magnetic layers, the transmission being larger when both the magnetic layers are aligned parallel to each other. The BEMM current in this case is two times higher in the parallel configuration than in the anti-parallel configuration.

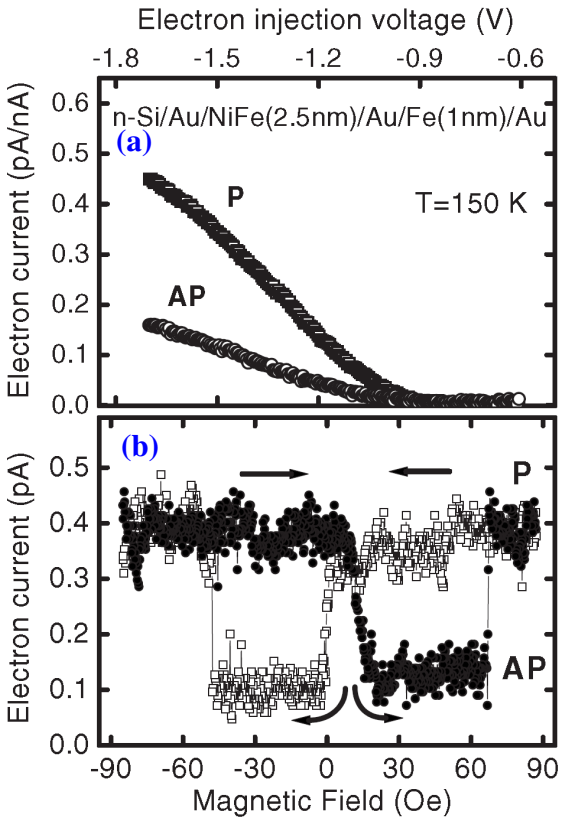

Figure 2.2 a) BEMM current versus tip-base bias in the spin valve device for parallel and anti-parallel magnetization geometries. b) BEMM current versus magnetic field at V_T = -1.7 V and an injection current of 1 nA at 150 K [14].

Part (b) of Figure 2.2 shows another type of measurement that has been performed by BEMM in this spin valve. In this measurement the tip is spatially fixed at a constant voltage and constant injected-current and the magnetic field is swept. The BEMM transmission is then recorded as a function of the magnetic field. A large drop in the BEMM current is seen when the magnetization of one of the ferromagnet changes with respect to the other, while the BEMM current is a maximum for a parallel orientation of the magnetizations of both the layers accompanied by a clear hysteresis loop.

2.5. Low Temperature Installation

One of the key characteristics of the BEEM system is its ability to perform measurements at different temperatures. This allows one to study the local differences in electrical transmission or magnetic behavior in magnetic multilayers as a function of temperature. To track and control the temperature dependence of the measurements in our BEEM system, a low temperature controller and sensors were installed during this project and liquid nitrogen was used to cool down the sample to 95 K. For more detailed information on the connections and silicon sensors see Appendix I.

Chapter 3: Experimental Techniques

In this chapter we describe various experimental techniques which were used to fabricate the devices beginning from a single crystal substrate of Nb:STO. We first describe the important characteristics of pulsed laser deposition technique and the other deposition technique namely sputtering, which was used for depositing Ti for making ohmic contact to the devices. Then we give a brief explanation of all the important systems that have been used for the characterization of bare substrates or *LSMO films or devices viz. physical property measurement system, atomic force microscopy, and low-temperature four-probe station. In the previous chapter, we already have discussed BEEM and its important characteristics.*

3.1. Pulsed Laser Deposition

Pulsed Laser Deposition (PLD) is categorized as a physical vapor deposition technique in which a high power pulsed laser beam is focused inside a vacuum chamber to strike a target of the material that is to be deposited. Figure 3.1 shows a schematic of a PLD system. The substrate on which material is to be deposited is heated up to some finite temperature, using a heater, before deposition is started. When the laser pulse strikes the target it is immediately absorbed by it and of different complex phenomena occur. The incident photon energy is converted into thermal and mechanical energy resulting in evaporation, ablation, and plasma formation. This plasma containing many energetic particles is directed towards a direction normal to the plane of the target. These energetic particles include atoms, molecules, clusters, and even molten globules, before depositing on the heated substrate. Particles from this plume are deposited on the substrate as a thin film. PLD can occur in ultra high vacuum or in the presence of a background gas such as oxygen, which is commonly used when depositing ferromagnetic oxides in order to fully oxygenate the deposited films.

The stoichiometry of the final deposited thin film is essentially the same as that of the target but the fundamental processes occurring during the transfer of material from target to substrate are not fully understood. However, the crystal quality depends mainly on the absorption, desorption, diffusivity, background gas, pressure, and power of the incident laser beam. For a more complete description of the PLD we refer the reader to reference [15].

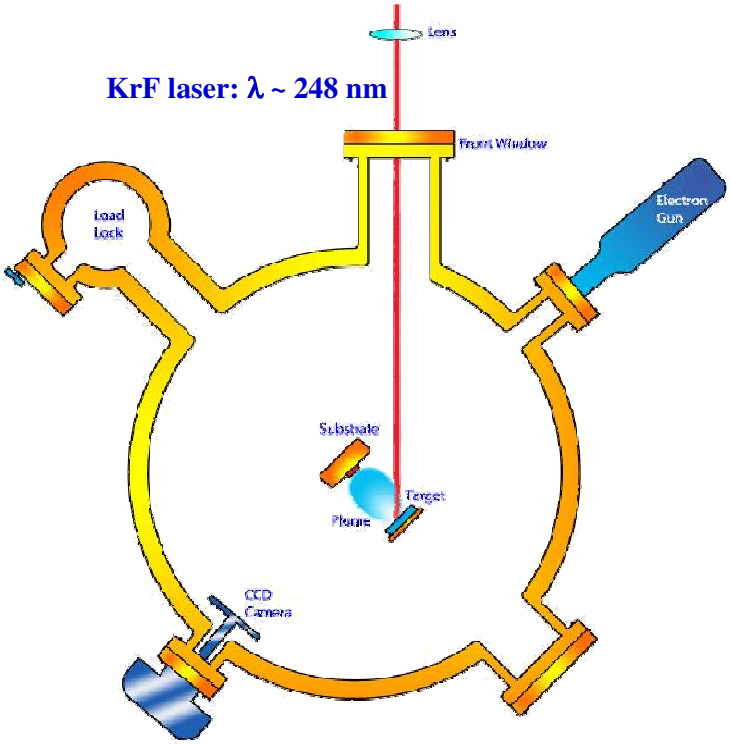

Figure 3.1 schematic representation of a PLD system. Pulsed laser is incident on the target and ejects particles, some of which end up depositing on the hot substrate.

Another positive point in utilizing a PLD system to deposit thin crystalline films is the possibility of using Reflection High-Energy Electron Diffraction (RHEED) as indicated in Figure 3.1. RHEED is a technique used for in situ characterization of the surface of crystalline materials. In this technique, information is gathered only from the surface of the sample after an accelerated electron beam generated in an electron gun, is incident on the surface at grazing angle (< 3 deg) and reflected. Upon reflection, electrons diffract and form a diffraction pattern on the phosphor screen or CCD camera. The shape of the pattern depends on the structure and the morphology of the probed surface (for details see [16]). Features in this diffraction pattern explain the surface structure and its crystallographic orientation. During the growth of thin film on a substrate, RHEED intensity shows an oscillatory pattern that determines the growth rate of the thin film. Using this property one can monitor layer-by-layer growth of the thin film.

3.2. Sputtering System

Sputtering is a process whereby atoms are stripped off from a target material via ion bombardment of the target and is commonly used for thin film deposition. In a sputtering system, first the neutral atoms in the chamber (in this case Ar) are ionized by electrons and then accelerated in a high electric field. These ions accelerate towards the target because of the existing potential difference. After collision, the incident ions set off cascade impacts in the target material. When cascaded atoms recoil and reach the target surface with energies above the surface binding energy, these atoms are ejected from the target. The average number of atoms ejected from the target per each incident ion is called the sputter yield. This type of sputtering is called DC-Sputtering (DC stands for

direct current) since in this case a DC voltage (~2 to 5 kV) is applied to target-substrate having the target biased in negative. There are also other ways in which plasma can be produced to eject atoms from the target. One of the most practical methods is RF-Sputtering (RF stands for radio frequency) which is used especially in deposition of insulating materials. This advantage comes from the fact that in an RF system there is no net current flow to either of electrodes, and therefore no charge buildup happens, while in a DC system the one-way nature of DC plasma causes a charge to buildup on the electrodes. Therefore, the RF sputtering technique is the best way to deposit an insulating layer, for example SiO_2. For more details on this deposition technique, we refer the reader to reference [17].

3.3. Atomic Force Microscopy

Atomic Force Microscopy (AFM) belongs to the Scanning Probe Microscopy (SPM) family in which a fine tip is brought into close contact with a sample surface without actually touching it. This is done by sensing the repulsive force between the probe tip and the surface in a technique called tapping mode. The order of magnitude of these forces is extremely small (around 1 nN). To create an image, the tip is scanned over the area of interest by moving back and forth over the sample surface. AFM can measure the topography with atomic resolution depending on the tip diameter and aspect ratio. AFM samples require no preparation, and they can be scanned in ambient conditions. The AFM system that we have been using in our studies has been Nanoscope IV, which was a product from Digital Instruments. For a complete description of this technique, the reader is referred to reference [18].

3.4. Physical Property Measurement System

The Physical Property Measurement System (PPMS) is an effective and powerful tool for measuring the electrical and physical properties of samples at extreme temperatures and/or magnetic fields. The maximum applicable magnetic field or temperature for different PPMS systems is different. In our case, the maximum applicable magnetic field was 3 Teslas (equivalent to 30000 Oersted) and the maximum feasible temperature was 350 K. The minimum temperature we could reach in our PPMS system has been approximately 2 K. A big advantage of PPMS is that complex measurements can be done with a minimum investment of the operator's time, since the whole measurement procedure is automated.

3.5. Low Temperature Probe Station

Low-temperature probe-station is an equipment that enables the operator to measure the I-V curve, conductance, and interface barrier heights at different temperatures. In this technique, soft Au probes are manually landed on the device's electrodes aided by powerful microscopes or cameras within an accuracy of almost 50 μm. Depending on the type of experiment, the operator may use two-probes (e.g. simple I-V), 3 probes (e.g. transistor), or 4 probes (for non-local I-V curve measurements).

Chapter 4: Characterization of Nb:STO Substrates

In this chapter, the results of the electrical characterization of the oxide substrates, which were used later in this project for fabricating diodes, will be presented. Since not much work has been done on understanding the transport mechanisms in oxide semiconductors, viz. Nb doped STO, it was imperative to study its resistivity, mobility, and carrier concentration at different doping concentrations, prior to using them as substrates for devices. We first give an explanation how contacts are made to the substrates and why it is so vital to obtain the correct contacts. Thereafter, we discuss the measurements that were done to determine the resistivity, carrier concentration and mobility of the charge carriers in these substrates at different temperatures. Finally, we compare our results with those of existing reports on similar systems.

4.1. Ohmic Contact

An ohmic contact between a metal and semiconductor is expected to yield a linear current-voltage characteristic. Ohmic contacts are a pre-requisite in any electronic devices when one is interested in extracting the physical properties of the material under investigation (viz. resistance etc.) without being influenced by the current leads. To make ohmic contacts on Nb:STO, several metals can be considered as electrodes, for example Au, Ti, Al, or Pt. Since during device fabrication, we go to high temperatures of up to 800°C, metal electrodes with lower melting points than this are not suitable. Besides, one should also take care that the work function of the metal electrode closely matches that of the Nb:STO substrate (~3.9 eV [19]). Satisfying both the above criteria i.e high melting point (~1650 ^{o}C) and a work function of ~4.33 eV, Ti has been found to be the best choice.

Ti was sputter deposited on a Nb:STO substrate and the I-V curve of one such contact is shown in Figure 4.1. This measurement was performed using the probe station at room temperature. From this graph we find the contact resistance is nearly 10 Ω which represents a good ohmic contact, as desired.

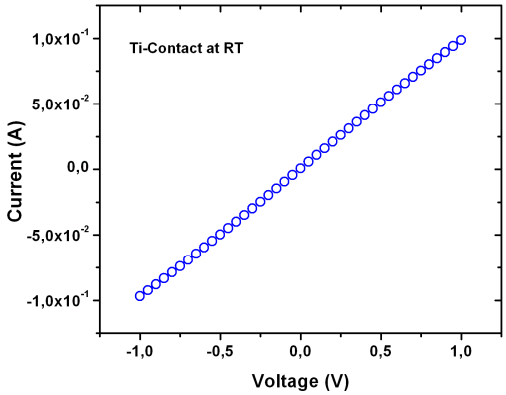

Figure 4.1 I-V curve showing ohmic behavior of Ti/Nb:STO contact, obtained from probe station.

4.2. Device Geometry

For all electrical measurements described in this chapter, we sputtered Ti contacts on top of a square shaped (5-10 mm^2) Nb:STO substrate. Ti contacts having 0.5 mm diameter and located 1 mm away from each other were sputtered on Nb:STO polished surface using a metal mask. The thickness of the sputtered Ti in all the measurements done for electrical characterization was 200 nm. To study the electrical properties of the substrates at different temperatures, we used both the probe station as well as the Physical Property Measurement System (PPMS). The advantage of PPMS over probe station, is that we can apply a magnetic field perpendicular to the substrate plane and thus extract parameters as resistivity, carrier concentration and mobility from the obtained Hall voltage. Independently, we can also determine the resistivity of the substrate using the probe station and compare it with the results obtained with the PPMS.

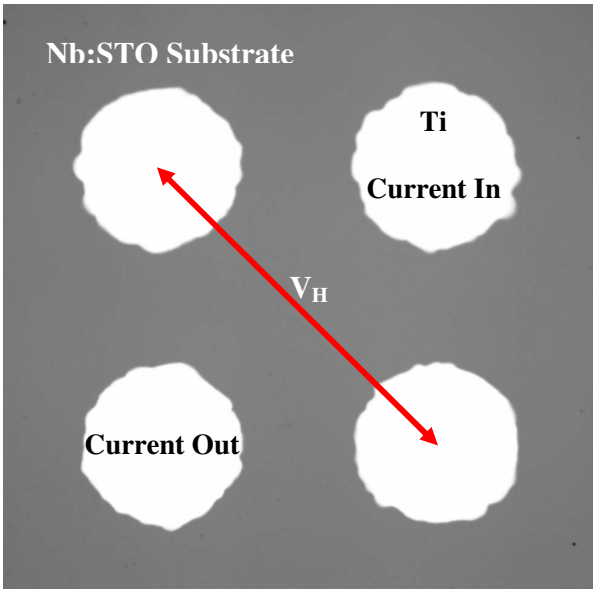

Figure 4.2 an optical top-view of the Nb:STO substrate after deposition of Ti contacts. Ti contacts were 0.5 mm in diameter, and were located 1 mm away from each other. Ti thickness was 200 nm.

An optical top-view of the device that was used in electrical characterization of Nb:STO substrate is shown in Figure 4.2. For resistivity measurements in the probe station any two contacts were used. To perform Hall measurements, four contacts were made on Nb:STO substrate as shown in Figure 4.2. Ti contacts on the surface of the Nb:STO were connected to a base-holder using aluminum-silicon ultrasone wire-bonds. This connected device was then inserted in a dipstick and introduced into a low temperature cryostat with the possibility to apply a magnetic field in a direction perpendicular to the plane of the substrate.
To measure the Hall voltage in our device, a current was sent into the substrate through one pair of diagonally opposite contacts and the voltage drop measured by the other pair using a Keithley meter, at different temperatures. The Hall voltage drop was measured between the other remaining two contacts, when an external magnetic field of 3 T was applied perpendicular to the substrate plane as shown in Figure 4.2. From this value of Hall voltage, carrier concentration and mobility of the substrates under investigation was determined.

4.3. Resistivity in Nb:STO Substrates

First, we used the probe station to determine the resistivity of our substrates with various Nb doping concentrations. A STO substrate having 0.01 weight percent of Nb doping (0.01 wt% Nb:STO) was chosen for the first characterization. Ohmic contacts were fabricated as discussed in the previous section. Measuring the I-V curves at various temperatures gives us the resistance of the substrate (R=V/I) at corresponding temperatures. Knowing the resistance, resistivity was easily obtained using the equation mentioned below.

$$\rho = R\frac{A}{L} \tag{4.1}$$

where, ρ is resistivity, R is the resistance, A is the area, and L is the distance between the electrodes. In our measurements A is assumed to be roughly $(0.5 \pm 0.05) \times (0.5 \pm 0.05)\ mm^2$ and the distance between two electrodes is 2±0.2 mm. The obtained resistivity-temperature dependence plot of 0.01 wt% Nb:STO substrate is shown in Figure 4.3. It is seen that by increasing the temperature from 210 K to 290 K resistivity increases from 3.6 to 6.1 mΩ-cm almost in a linear fashion.

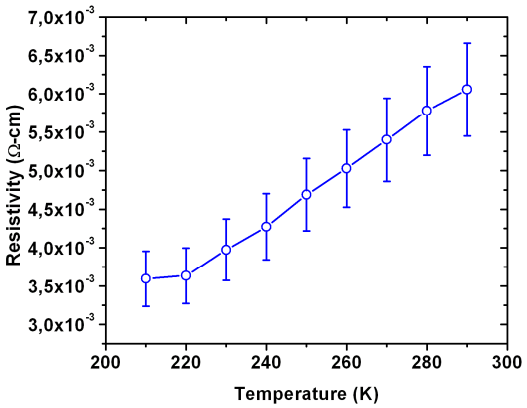

Figure 4.3 dependence of resistivity on temperature related to a 0.01 WT% Nb:STO substrate. In this graph, resistivity increases in a linear fashion with increasing temperature.

Similar electrical characterization of Nb:STO substrates with higher Nb doping viz. 0.05 wt% and 0.1 wt% were done and were later used as substrates for the devices described in Chapters 5 and 6. PPMS was used for the electrical characterization. To measure resistivity in PPMS, I-V was measured from four fabricated contacts as described in section 4.2. Figure 4.4 shows their resistivity-temperature dependence plot. Part (a) shows resistivity-temperature dependence for the 0.05 wt% Nb:STO substrate while part (b) shows the same for 0.1 wt% Nb:STO substrate. In both graphs, a clear increase in resistivity of the substrate is seen with increasing temperature. At room temperature, the resistivity for the 0.05 wt% Nb:STO substrate is ~2.4 mΩ-cm and ~0.54 mΩ-cm for the 0.1 wt% Nb:STO substrate.

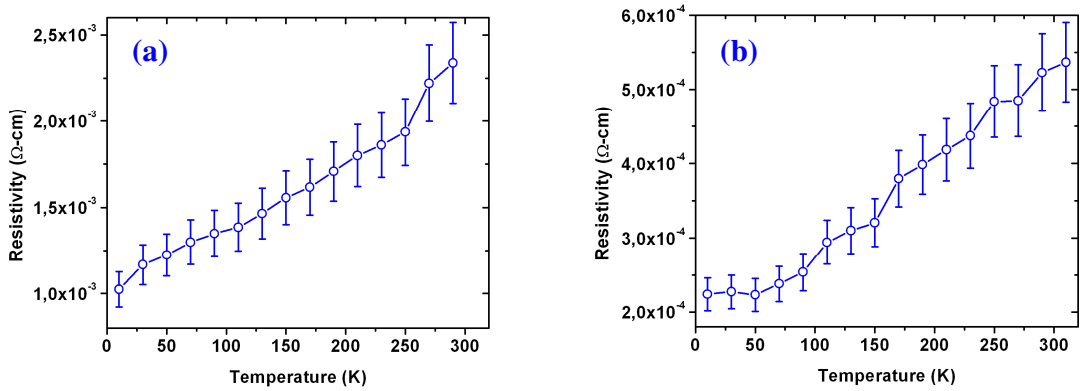

Figure 4.4 resistivity versus temperature for a) 0.05 WT% Nb:STO and b) 0.1 WT% Nb:STO substrates.

By comparing the graphs in Figure 4.3 and Figure 4.4 (a) and (b), it is clear that an increase in the Nb doping leads to a decrease in the resistivity, as expected. Increasing the Nb doping by 5 times (i.e. from 0.01 wt% to 0.05 wt% Nb:STO), causes the reduction of the resistivity of Nb:STO to half its value (both at RT and LT) whereas, increasing the doping concentration by 10 times (i.e. for 0.1 from 0.01 wt% to 0.1 wt% of Nb:STO), leads to a reduction in the resistivity by an order of magnitude. The general trend and the

values that we have obtained in this study are in good agreement with what has been reported, so far, in other publications [20].

4.4. Carrier concentration in Nb:STO Substrates

As part of electrical characterization of the substrates, the carrier concentration of the substrate and its dependence on temperature was studied. For this, we performed Hall measurements as described in section 4.2. We applied the field in a direction perpendicular to the plane of the substrate and measured the Hall voltage. No special Hall bar geometry was used for measuring the Hall voltage. Once the Hall voltage is measured and we know the corresponding applied current, the carrier concentration can be easily calculated from the following equation.

$$n = \frac{I\,B}{e\,d\,V_H} \qquad 4.2$$

where n is carrier concentration, I the current, B the applied magnetic field, e the absolute value of electron charge, d the thickness of the substrate, and V_H the Hall voltage. We applied a 3 Tesla (T) field in a direction perpendicular to the plane of substrate. Substrates of thickness 0.5 mm were used. The measurement of V_H at fixed magnetic field and known current was performed at various temperatures. Hence, using above mentioned equation the carrier concentration versus temperature was obtained as shown in Figure 4.5. These plots have y axis in logarithmic scale. Figure 4.5 (a) corresponds to 0.05 wt% Nb:STO and (b) corresponds to 0.1 wt% Nb:STO substrates. It can be clearly observed from this figure that with the increase in temperature, the carrier concentration decreases.

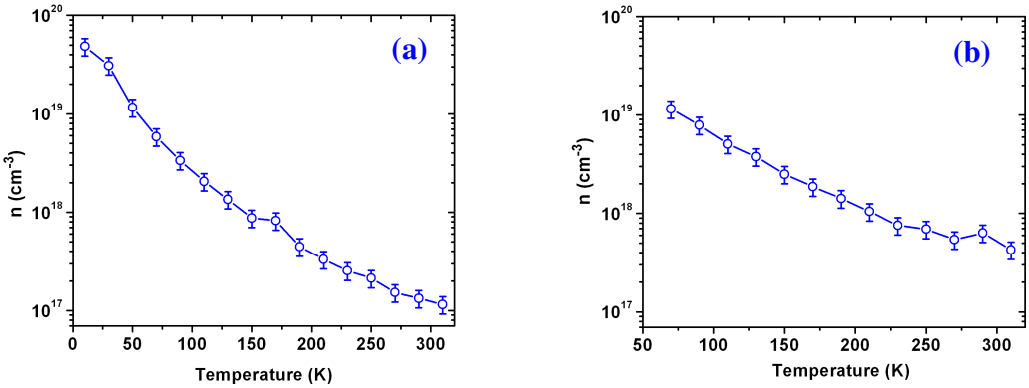

Figure 4.5 carrier concentration versus temperature for a) 0.05 wt% Nb:STO and b) 0.1 wt% Nb:STO substrates.

By comparing the graphs in Figure 4.5 at RT as well as LT, we observe that increasing the doping concentration of Nb leads to an increase in carrier concentration in these

substrates. Thus, by increasing the carrier concentration, by 2 times (i.e. from 0.05 wt% to 0.1 wt% Nb:STO), the carrier concentration at RT increased approximately six times (i.e. from $10^{17} \pm 1.1 \times 10^{18}\, cm^{-3}$ and $6 \times 10^{17} \pm 1.2 \times 10^{18}\, cm^{-3}$).

4.5. Mobility in Nb:STO Substrates

Knowing the values of resistivity and carrier concentration at various temperatures, we can calculate the mobility of the substrates using the equation 4.3.

$$\mu = \frac{1}{\rho n e} \qquad 4.3$$

where μ represents the mobility. Figure 4.6 (a) and (b), (y axis log scale), compares the mobilities of 0.05 wt% Nb:STO and 0.1 wt% Nb:STO substrates with increasing temperature. Since the mobility is directly calculated from the resistivity and the carrier concentration, it is foreseen that the general trends in these graphs are directly affected by those in Figure 4.4 and Figure 4.5.

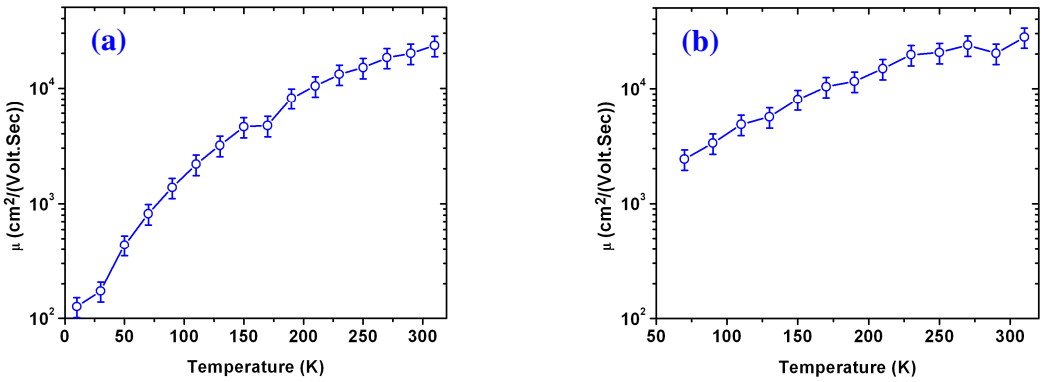

Figure 4.6 mobility versus temperature for a) 0.05 wt% Nb:STO and b) 0.1 wt% Nb:STO substrates.

4.6. Discussion

The changes in resistivity values for the semiconducting Nb:STO substrate, at different temperatures, are in good agreement with our expectations and also with other reported results [20]. We have seen that by increasing the niobium content of the substrates, resistivity decreases. However, slight differences exist between the obtained trends in the carrier concentration with temperature in our case as compared to that of other published results. Whereas we find the carrier concentration to decrease by two orders of magnitude with increasing temperature for both the doping concentrations, literature reports indicate an almost constant value [20]. This also leads to differences in the value of the mobility in our experiments, as the mobility is calculated directly from the resistivity and the carrier concentration. We believe that the origin of this discrepancy might be in the

device geometry that we have used for measuring the Hall voltage. The most commonly used geometry to measure the Hall voltage is the Hall bar or Hall cross geometry. Whereas published literature reports do use this geometry, we did not, as this was outside the purview of our work. However, we plan to do this at a later time to verify if this proposition is correct.

Nevertheless, an important issue needs to be discussed here, namely the increasing nature of the resistivity with increasing temperature in Nb:STO substrates. This unique phenomena has not been negated by any of the research groups working with Nb:STO. While, Tufte *et al* [20] tried to relate this decrease in resistivity of Nb:STO to the bulk of the substrate at low temperatures, lately, Susaki *et al* [21] [22] have attempted to address this issue in a completely different way. They suggested that the low temperature behavior of Nb:STO is not a property that comes from the bulk, but is a pheomenon that originates at the metal/Nb:STO interface. In their opinion, the permittivity of the Nb:STO at the interface with a metal contact (within 5 nm distance from interface) decreases with decreasing temperature, as opposed to the permittivity of the Nb:STO bulk which increases. Thus we have to account for the largely unknown complexities of the metal/Nb:STO interface before we can draw specific conclusions regarding the electrical properties of these doped oxide substrates.

Chapter 5: Structural, Magnetic and Electrical Characterization of Fabricated LSMO/Nb:STO Diodes

This chapter gives a detailed account of the fabrication and characterization of the LSMO/Nb:STO diodes. Very little is known about the interface between typical half metallic ferromagnets and non-conventional semiconductors such as doped STO. However, such diodes are the building blocks of any electronic device and hold great promise for oxide spintronics devices. The fabrication protocol of the diodes, the challenges faced and the obstacles surmounted in optimizing the fabrication protocol have all been described in different sections of this chapter. The characteristics of the half-metallic LSMO layer deposited by Pulsed Laser Deposition and the optimization of its various parameters for efficient working as diodes are also discussed. The structural and magnetization properties of the deposited layers is presented as well. Finally, the results and analysis of the electrical characterization of the fabricated diodes using two probe measurements at the probe station and BEEM system are discussed.

5.1. TiO_2 Termination of the Surface

It is widely known that LSMO grows epitaxially on lattice matched STO substrates. However, as received substrates have to be free of surface contaminants and should be properly terminated at the surface so as to facilitate such an epitaxial growth. As received Nb:STO substrates are polished on one side. The active area of the device will be fabricated onto these polished sides. The surface of as-received STO substrate consists of both the sublattices of TiO_2 and SrO as is shown in Figure 5.1 (a). A chemical treatment is necessary to ensure that the top surface has a single termination, preferably that of TiO_2. Such a termination is also a natural choice as it is calculated to have the lowest surface energy [23] enabling the epitaxial growth of the LSMO layer.

The chemical treatment process takes advantage of the differences in the solubility of both the sublattices in acids. First the substrate is sonicated in deionized (DI) water for 30 minutes. This hydrates the SrO planes at the surface in the following manner $SrO + H_2O \rightarrow Sr(OH)_2 + H_2$. $Sr(OH)_2$ is then removed by a quick dip (30 s) in ultrasonicated BHF (Buffered HF) (pH=5.5) which generates $Sr(OH)_2 + 2HF \rightarrow SrF_2 + 2H_2O$. Further residues are removed by rinsing in an ultrasonic bath of DI followed by ethanol. This leads to a TiO_2 termination of the top surface of the STO substrate.

Figure 5.1 (a) and (b) are the tapping-mode AFM images (scan size 5 x 5 μm^2) of a 0.1 wt% Nb doped STO surface, before and after termination. Figure 5.1 (b) represents the unit cell terrace steps at the STO surface.

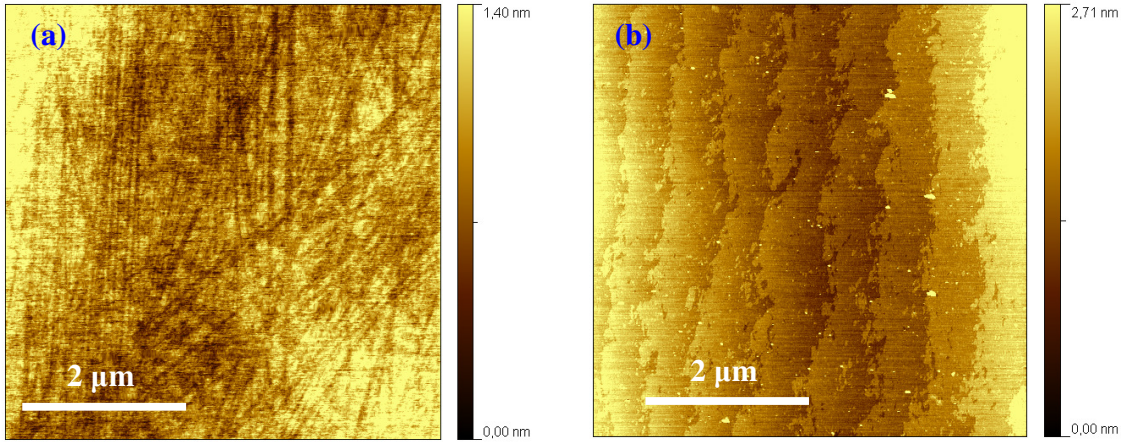

Figure 5.1 a) AFM images from the surface of an as received 0.1 WT% Nb doped STO substrate. b) AFM picture of the same substrate after chemical treatment.

5.2. Annealing

To obtain crystalline perfection of the top surface, ideal for the epitaxial growth of the LSMO layer, the substrates are then annealed. Annealing is done at 960°C for nearly 2 h in the presence of oxygen (O_2 flow in our annealing system was kept between 250 and 300 sccm). Annealing gives the unit cells, on the surface of the substrate, enough time and energy to relocate onto areas in which they are more stable. In practice, this stability issue is translated into smoother and straighter terraces.

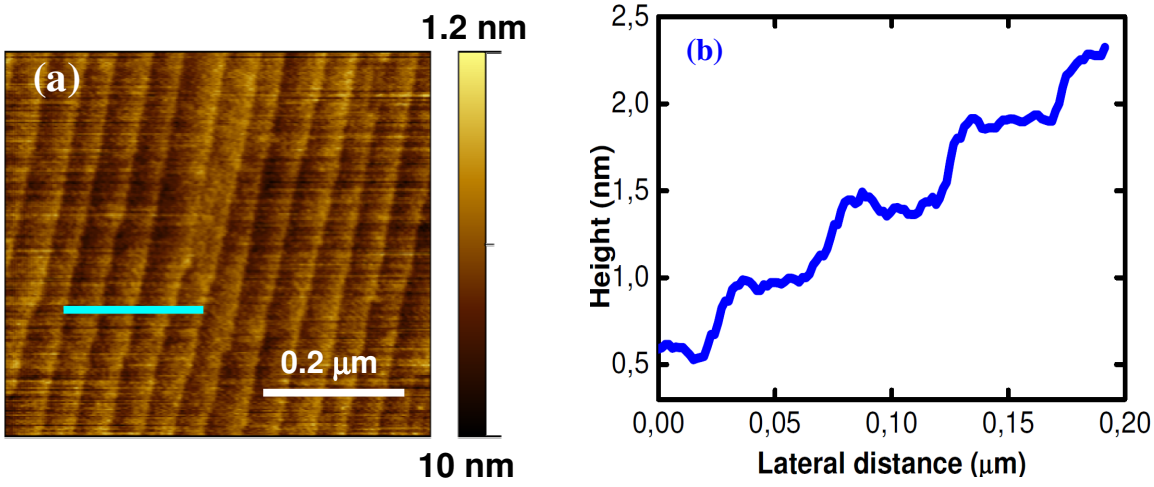

Figure 5.2 AFM image (a) and step height profile (b) of a substrate after chemical treatment and annealing. It shows clean terraces having ~0.38 nm step heights corresponding to one unit cell height.

An AFM picture of a chemically treated and annealed substrate is shown in Figure 5.2 (a). In part (b) of the same figure, the step height profile is shown. This profile shows step

heights of 0.38 nm corresponding to one unit cell height for each of the terraces. Such a terminated TiO_2 substrate top surface is well suited for LSMO deposition.

5.3. Back-Contact Deposition

The sample for the BEEM studies should consist of a large contact to the semiconducting substrate so as to collect the transmitted electron current. Such back-contacts for conventional Si substrates are easily realized depositing either Au or Ti/Au or Cr/Au. The large area of the contacts ensures that good ohmic contacts are formed at the Si surface in combination with these materials. However, for the case of oxide semiconducting substrates as Nb:STO, the situation is somewhat different. It has been reported that Au readily forms a Schottky diode (SBH=1.4 eV) with Nb:STO substrate even for large areas (~ 1 mm^2) [21]. Further, since the fabrication of the diodes involves a few heating steps (also in the presence of oxygen flow), diffusion of the deposited metallic layers is highly probable as is their oxidation. We ran into few problems looking for the proper combination of materials and also identifying the step in the fabrication protocol when such metallic contacts can be made to the semiconducting substrate. Throughout this thesis, we have used sputtering to deposit our large area metal contacts. After a few trial diode fabrication and characterization, we finally solved the challenging back-contact problem. 300 nm of Ti followed by 200 nm of Au were used as our back contacts. Both these materials were deposited using our sputtering technique at the Nanolab. We also radically changed the fabrication step at which the back contacts needed to be sputtered. It was found that to overcome issues related to oxidation of the contacts at the substrate annealing temperature of 960°C (each time for almost 2 h) and involving oxygen flow, the back contacts are best sputtered just before the PLD deposition of the LSMO layer.

5.4. Lithography

Figure 5.3 represents an overall geometry of the final device. Optical lithography has been used to realize the active area of the device. To obtain negative resist sidewalls, (See Appendix II for details) which inhibits the coverage of coated films onto the resist sidewalls and makes lift-off processes more reproducible and stable, an image reversal photo resist TI35ES was used. Such a step is necessary when we want to minimize the active area of the diode and to isolate it from the rest of the substrate. The active area is 150 μm in diameter in our case (see Figure 5.3) and isolated from the rest of the substrate by a thick SiO_2 insulating layer. Details of the sputtering of the SiO_2 are mentioned in the next section.

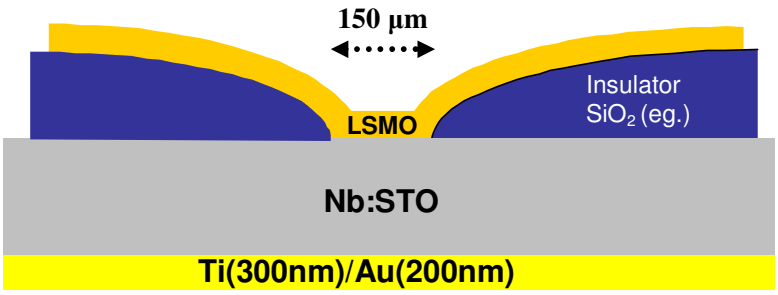

Figure 5.3 schematic representation of the final device. Active area comprises of 150 µm diameter cavity inside the SiO_2 insulator. It is clear that only at the active area LSMO layer meets the substrate.

5.5. Optimization of the Insulating SiO_2 Layer

One of the essential parts in the device fabrication involves forming a relatively thick, highly insulating, pin hole free SiO_2 layer (see Figure 5.3 for the device geometry). Although the best stoichiometric SiO_2 layers are obtained by dry or wet oxidation of a Si wafer, clearly for this project this process is unsuitable. We thus used sputtering to grow such a layer. Sputtering usually leads to a SiO_2 layer with good insulating properties, but is often defect-ridden, thus the normal breakdown of the insulator can occur even at a relatively low bias of 5 V. This is also not wanted for our studies as will be clear in Chapter 6. A key contribution of this project was to establish a protocol, to grow reproducibly thick SiO_2 layers with good insulating properties and capable of withstanding a large bias at least up to 10 V. This was successfully implemented but involved quite some time. Today, this protocol is successfully used by other groups at the Zernike Institute. A number of deposition parameters in the sputtering system needed to be optimized and a few shadow masks were designed for this purpose. Knowing that the quality of the deposited silicon dioxide layer is a direct result of the trade off between chamber pressure, oxygen to argon ratio, target to substrate distance, RF power, substrate material and temperature, it was not an easy job to find out the optimized parameters of deposition specific to our sputtering system.

In this regard, we performed different experiments to find out the best deposition parameters in our sputtering system. A separate sub-project was undertaken to establish the insulating nature of the SiO_2 oxide layer. The device geometry for this purpose involved shadow masks and is shown schematically in Figure 5.4 (a). Top and bottom electrodes have been made through deposition of few hundred nanometers of Ti and in some cases were capped by Au. Titanium was our preferred electrode choice because of its relatively hard surface that could better support the metal probes in the probe station. In part (b) of the same figure, an optical image of a corner of one of the devices is shown. To measure the electrical properties of our devices, two clean tips of probe station system have been gently placed at each end of the top and bottom electrodes. To make sure that there was no current passing through the substrate, a Si/SiO_2 (300 nm) insulating substrate was used.

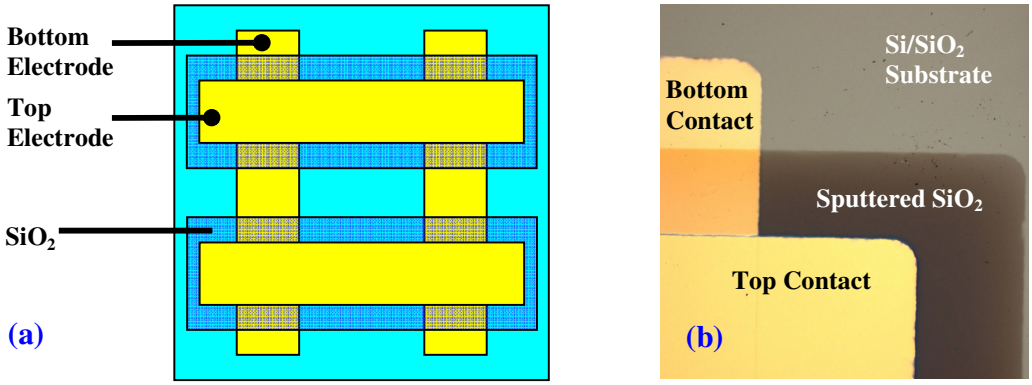

Figure 5.4 a) schematic representation of the geometry by which the insulating strength of deposited SiO_2 layer has been investigated. b) an optical view of top corner of one of the devices. Two yellow parts indicate the electrodes that have sandwiched the darker SiO_2 layer.

The parameters for which SiO_2 deposition yielded the desired result in our sputtering system have been mentioned in Table 5.1. With these values, oxygen makes up 15 % of the volume of the gas inside the chamber while argon fills the remaining 85 % of the volume.

Table 5.1 Optimized SiO_2 parameters that results in favorable insulating strength.

Chamber Pressure	RF Power	Ar Flow	O_2 Flow
7.0×10^{-6} bar	200 W	11 SCCM	2 SCCM

Figure 5.5 shows a tapping-mode AFM image of the sputtered SiO_2 (grains) along with I-V measurements of the same sample at room temperature. Figure 5.5 (b) shows the current flowing through the device up to a bias of 10 V. Sudden up and down changes in the current record shows that the measurements have been done outside the optimized working range of the probe. First, we see that our sputtered SiO_2 is capable of withstanding a bias of 10 V (even after 5-6 repeated cycling) and secondly the sputtered oxide is quite insulating, the resistance being almost 1 GΩ.

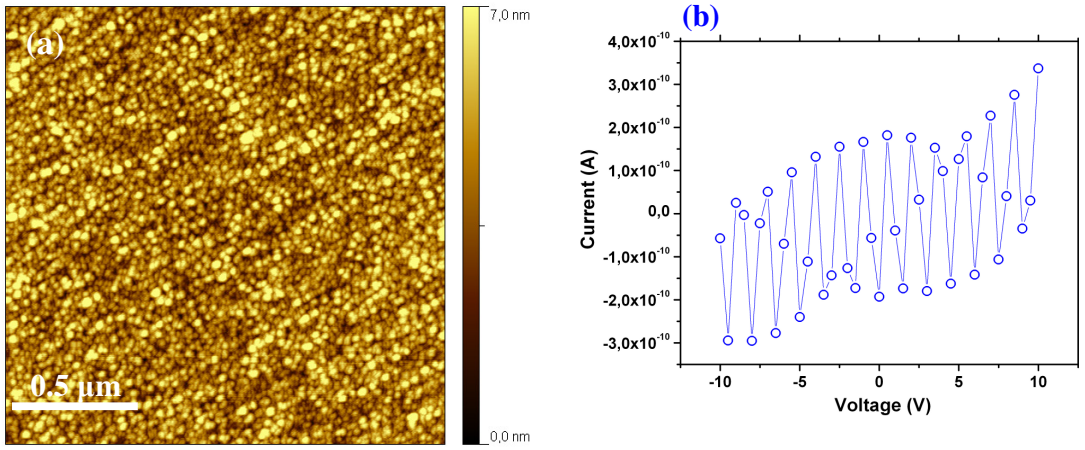

Figure 5.5 a) SiO_2 grains sputtered on Nb:STO substrate. b) the I-V curve showing good insulating strength of nearly 170 nm thick SiO_2 layer up to 10 V.

In a separate set of experiments, the actual thickness of the sputtered SiO_2 was also measured. The thickness of SiO_2 for the above conditions as mentioned in Table 5.1 is 170 nm. This was deduced from AFM step-height analysis of a substrate sputtered with SiO_2 and removal of the SiO_2 from selected area using an optical mask and BHF. Figure 5.6 (a) shows an AFM picture of the sputtered SiO_2 on Si/SiO_2 substrate after one hour of deposition. In part (b) the sharp step height profile indicates a nearly 217 nm thick SiO_2 deposited for this duration of time. The rate of SiO_2 deposition for this substrate is approximately 3.6 nm/min.

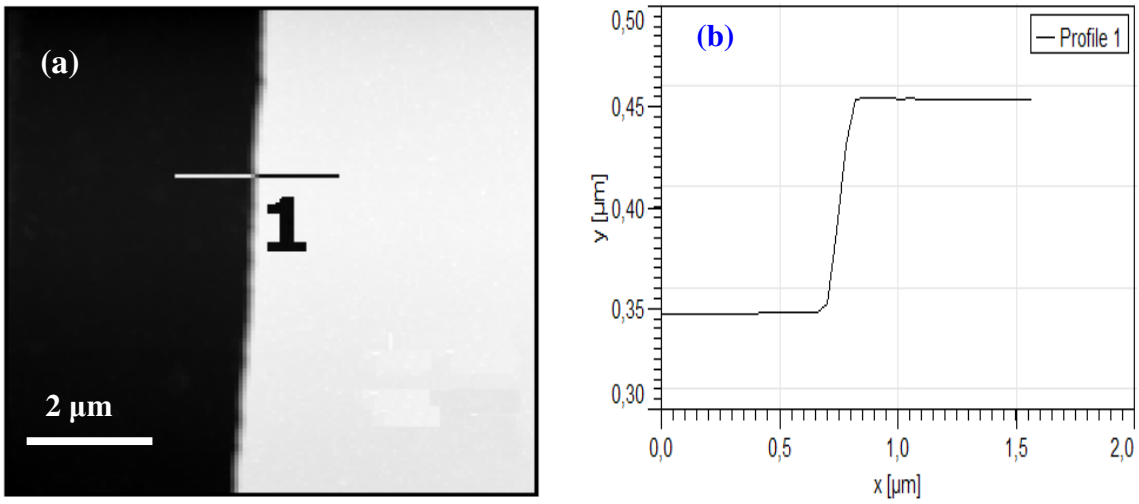

Figure 5.6 a) SiO_2 sputtered on Si/SiO_2 substrate. b) the step height profile showing ~217 nm of SiO_2 deposition after 1 h indicating a deposition rate of 3.6 nm/min.

5.6. Defining the Actual Device Area by Lift-Off

In previous two sections, we have discussed how we defined the active area of the device using optical lithography and thereafter sputtered SiO_2 on the entire substrate. In this section, we continue our device fabrication recipe by explaining how we lifted off the photoresist/SiO_2 from the device area. Lift-off of the resist in the active area is done by placing the substrate in an ultrasonic bath containing acetone. This process is quite long and might take anywhere between 60-90 minutes depending on how hardened the resist is. Intermittent checking of this was also done using optical micrograph and the Scanning Electron Microscope (SEM). To see how efficiently photoresist can be removed from the active area we coated the sputtered SiO_2 with Ti (100 nm)/Au (50 nm) and looked at the edges using SEM. Figure 5.7 (a) shows an optical microscope image of the 150 µm diameter active area after one hour of lift-off, while Figure 5.7 (b) shows a zoomed-in SEM picture of the edge surrounding the active-area.

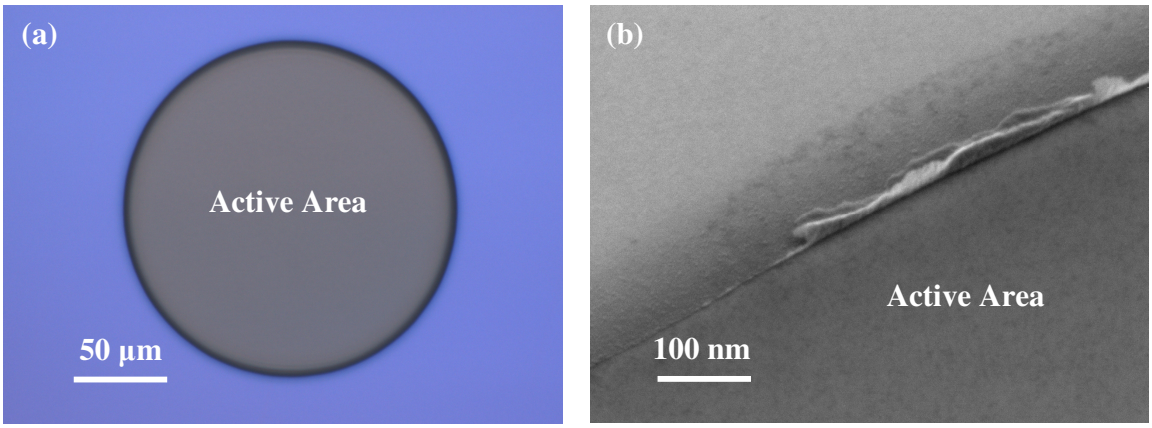

Figure 5.7 a) Microscope image of the active area after one hour of ultrasonication in acetone. b) SEM image from the edge surrounding the active area.

Remains of the photoresist can be easily spotted in Figure 5.8 (b) that shows a zoomed-in image of the active-area edge in Figure 5.8 (a). An effective way to clean the edges from photoresist is to increase the sonication time. However, we have seen that this highly affects the order of the terraces to the extent that after 5 h terraces can hardly be seen. Nevertheless, fortunately there is multiple-aspect solution to this problem that allows decreasing the sonication time in exchange for introduction of an additional step in the device-fabrication recipe. The newly introduced step is annealing (we call this step re-annealing from now on) that has multiple benefits. While it keeps the lift-off step short (one hour is enough), re-annealing effectively takes away the photoresist residue and restores the overall pattern of terraces. Also, annealing at this stage helps in transforming SiO_x components of the deposited silicon dioxide into SiO_2 [24] and therefore provides a more reliable insulating layer before LSMO is deposited. Figure 5.8 compares the AFM pictures of an active area (after 2 h of lift-off) on the 0.1 wt % Nb:STO substrate before and after re-annealing. Note that re-annealing conditions are the same as what was mentioned in the section 5.2, namely 960 ^{o}C for nearly 2 h in the presence of oxygen.

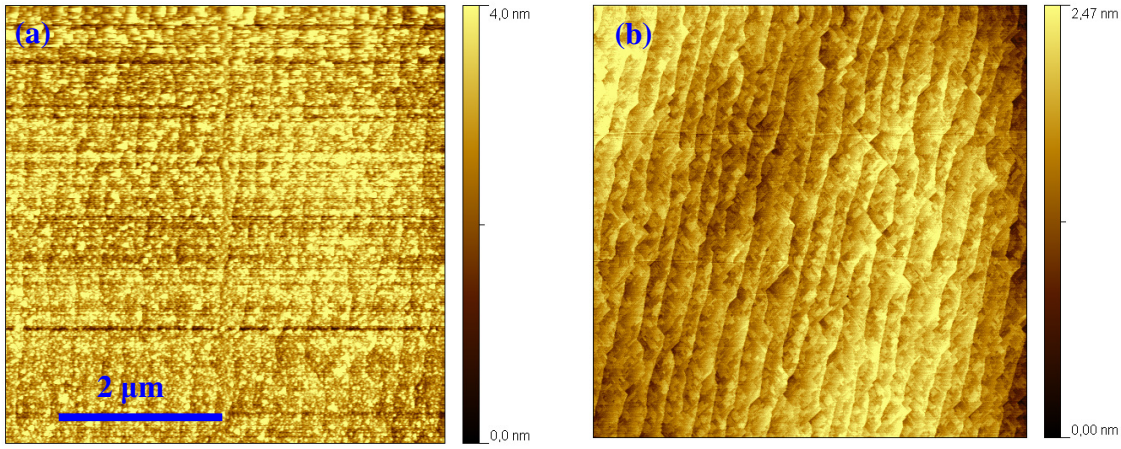

Figure 5.8 a) AFM image of the active area of an 0.1 WT% Nb:STO substrate after 2 h of ultrasonication in acetone. b) Surface of the same sample after undergoing a re-annealing step.

The thickness of the sputtered SiO_2 for the actual device was also measured and is shown in Figure 5.9. AFM step-height profile shows the thickness of the SiO_2 layer, in this case to be ~340 nm. The substrate in this case is 0.1 WT% Nb doped STO and the SiO_2 was sputtered for 2 h. From these values a deposition rate of nearly 2.83 nm /min is obtained, which compares well with the rate of 3.6 nm/min obtained on Si substrates (previous section).

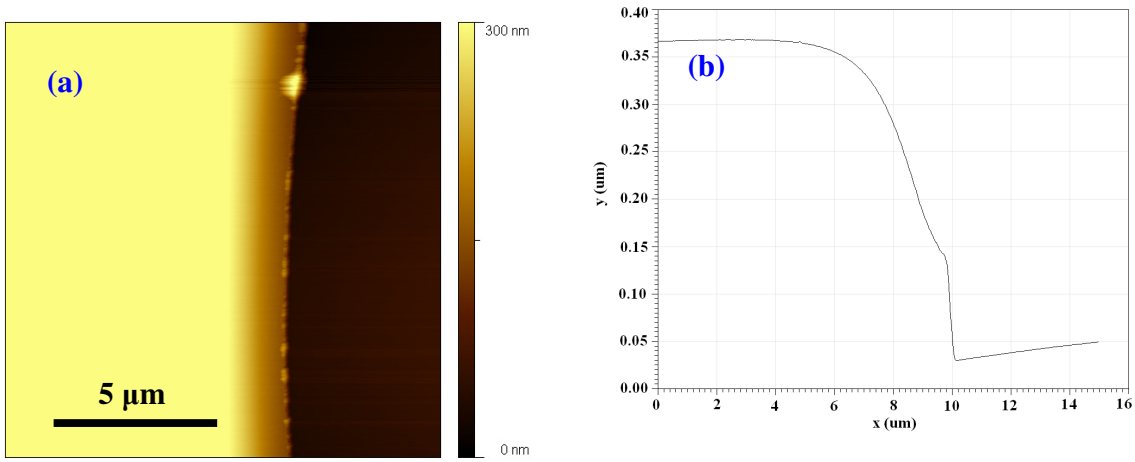

Figure 5.9 a) AFM image covering both the active area (dark) and SiO_2 layer on a 0.1 WT% Nb doped STO substrate. b) height profile of the same AFM image showing a nearly 340 nm thickness for SiO_2.

5.7. Pulsed Laser Deposition of LSMO

LSMO thin films were deposited on the patterned active-area of the substrate using PLD technique, as is shown in Figure 5.3. The PLD setup in Prof. Dr. B. Noheda's lab was used. While PLD is known to reproduce the stoichiometry of the target very well and thus is very suitable for the deposition of complex oxide materials, several parameters play a

vital role in the formation of a stoichiometric film. A homogeneous deposition results from a controlled trade-off between laser fluence, target to substrate distance, oxygen pressure, and substrate temperature. To add more to the complexity, one should bear in mind that the frequency of the laser pulses and post-annealing (annealing after LSMO deposition) are also deciding factors influencing the quality of the deposited film. Since no prior expertise existed regarding the growth of the LSMO film, a considerable amount of time was spent in optimizing the growth conditions so as to achieve well-stoichiometric films of LSMO.
To optimize and obtain the best parameters regarding LSMO deposition, specific to our PLD system, we have played with all the aforementioned variable parameters. Optimized LSMO deposition parameters, in the PLD system, suitable for LSMO film growth, are summarized in Table 5.2.

Table 5.2 Optimized LSMO deposition parameters for our PLD system.

Substrate Temperature	Laser Frequency	Oxygen Pressure	Laser Fluence	Target-to-Substrate	Post-Annealing
750 ^{o}C	1 Hz	0.35 mbar	1.8-2 J/cm^2	40 mm	> 60 minutes

It must be noted that LSMO deposition, using these parameters, yields one sixth of a monolayer of LSMO per each laser pulse. Knowing the fact that each monolayer has a 0.38 nm height, to grow, for instance 38 nm of LSMO, one should run the PLD for 10 m.

5.7.1 X-Ray Diffraction Studies of LSMO Films

To ensure the epitaxial growth of the LSMO film, X-Ray Diffraction (XRD) studies were performed on a 10 nm thick LSMO film deposited on STO substrate. The structural analysis was done separately for the substrate (STO) and for the film on the substrate (LSMO/STO). Figure 5.10 (a) shows a comparison between STO and LSMO/STO XRD data. In this figure blue lines represent the data for the LSMO film on STO while red lines correspond to the bare STO substrate. In the figure, the expected Miller indices (hkl) are attributed to the corresponding peaks. Figure 5.10 (b) shows a zoom in at the position of (002) peak in graph (a).

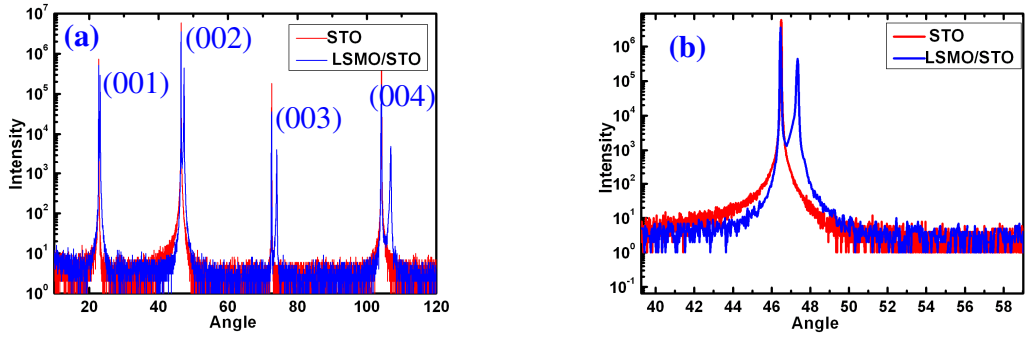

Figure 5.10 a) large angle XRD results of STO (red line) and LSMO/STO (blue line). b) zoom-in at (002)

peak of graph (a).

The following equations are used to calculate the lattice parameters once the Miller indices are known.

$$\frac{1}{d^2} = \frac{h^2 + k^2}{a^2} + \frac{l^2}{c^2} \qquad 5.1$$

$$2d \sin\theta = n\lambda \qquad 5.2$$

Using these equations and any of the Miller indices (00l) mentioned in Figure 5.10 (a) (along with their corresponding θ angle), the LSMO lattice parameter can be calculated. In our case, the out of plane lattice parameter c, for LSMO, using the above equations was calculated to be nearly 3.83±0.15 A. From these graphs a lattice mismatch of ~1.7 % between LSMO and Nb:STO is calculated.

5.7.2 Magnetic Properties of the Deposited LSMO Films

The magnetic properties of the as deposited films were also characterized using a Superconducting Quantum Interference Device (SQUID). The Curie temperature (the temperature at which LSMO film changes from ferromagnetic to paramagnetic phase) was determined and the coercivity of the deposited LSMO film estimated. Figure 5.11 (a) shows the magnetic moment of a 40 nm thick LSMO film versus temperature at 1000 Oe. This figure provides a proof that at room temperature LSMO film is still ferromagnetic, since its Curie temperature is above 300 K. In Figure 5.11 (b) the hysteresis loop of a 40 nm thick LSMO at 200 K is shown. In this figure at zero magnetic field a 10 Oe separation exists between two coercive points as it is shown in the inset to graph (b). This narrow separation indicates the soft nature of the LSMO thin film ferromagnet.

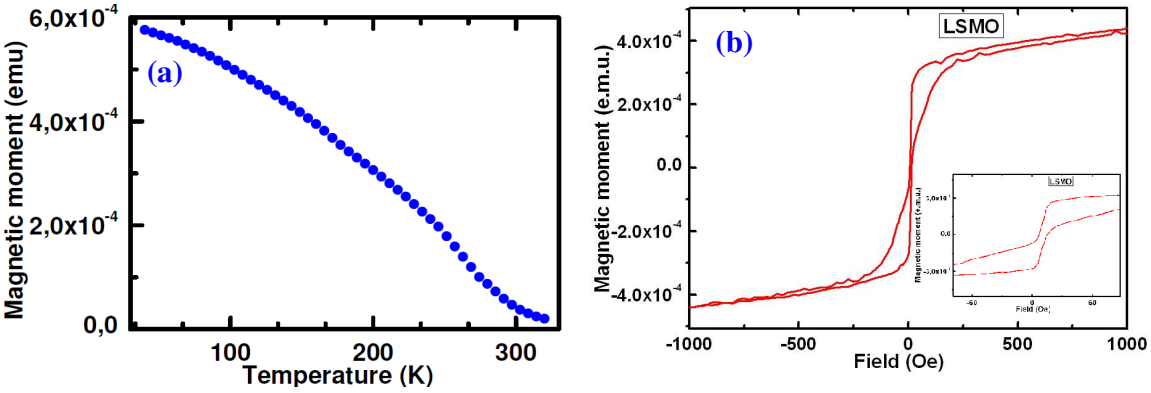

Figure 5.11 a) magnetic moment of the 40 nm thick LSMO layer versus temperature at 1000 Oe. It shows that the Curie temperature is higher than 300 K. b) magnetic moment of a 40 nm thick LSMO versus magnetic field at 200 K. A 10 Oe separation in left and right coercive points is shown in the inset.

5.7.3 Scanning Tunneling Spectroscopy Studies

A quick Scanning Tunneling Spectroscopy (STS) measurements was done on the deposited LSMO film. We have used the Platinum-Iridium STM for this purpose. The injected tunnel current is 1 nA and the applied bias is swept between -1 to +1V while the feedback loop to the tip was switched off. Apart from throwing light into the local density of states at the top LSMO layer, it also gives a rough estimate of the conductance of the top layers. Figure 5.12 shows an STS plot that has been obtained from a 9 nm thick LSMO grown on Nb:STO substrate. In between a bias from -0.4 to +0.4 V, very little current flows into the layer, thus indicating zero conductance and energy gap.

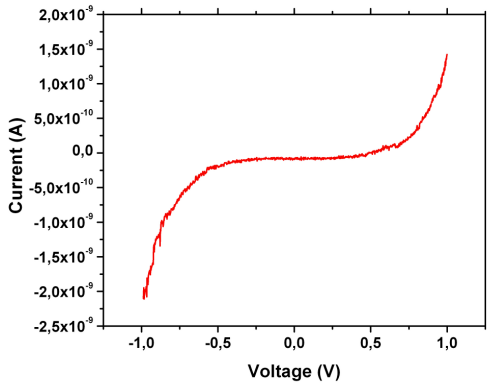

Figure 5.12 STS plot obtained from experiments on a 9 nm thick LSMO deposited on Nb:STO substrate.

5.8. Electrical Characterization of the LSMO/Nb:STO Diodes

Two-terminal I-V characterization of the fabricated LSMO/Nb:STO diodes was done at varying temperatures and will be presented next.

First, the resistance of the LSMO film was measured using a Keithley multimeter at RT and is shown in Figure 5.13. A clear ohmic behavior is observed that implies that the LSMO film is quite well conducting at RT (resistance 1 MΩ). However, the LSMO films are known to exhibit a temperature dependent resistivity, increasing with decreasing temperature. We have not explicitly performed this in our work but do see such a trend in our temperature dependent I-V and BEEM measurements.

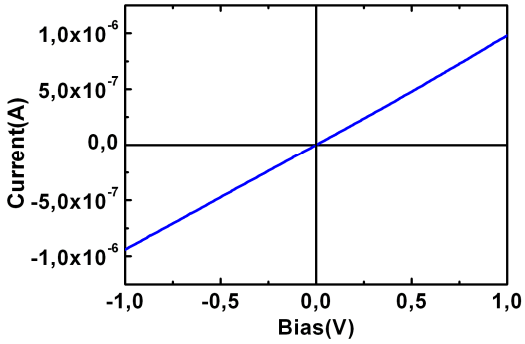

Figure 5.13 I-V curve describing the ohmic behavior of LSMO while it is in contact with metallic probe tips. Probes are placed ~0.5 cm away from each other and thickness of the LSMO is 9 nm. At one volt, the current is nearly 1 μA giving a resistance of 1 MΩ.

In the next few section we will present the results and analysis of the electrical characterization done on three different LSMO/Nb:STO diodes. For this project, 12 diodes have been prepared but we have chosen to present the characteristics of only three of them either because they are the most promising or because they gave some interesting threads on which further work can be pursued or has been pursued. The sequential information on the fabrication of these diodes is given in Table 5.3.

Table 5.3 Characteristics of diodes 1, 2, and 3. The numbers on the left show the sequence of the steps.

Steps	Characteristics		Diode 1	Diode 2	Diode 3
1	**Substrate**		0.01 WT% Nb:STO	0.05 WT% Nb:STO	0.1 WT% Nb:STO
2	**Back-Contact**		Ti (200 nm)/Au (5 nm)	Ti (200 nm)/Au (100 nm)	-
3	**Chemical Treatment**		Done	Done	Done
4	**Annealing**		1:56:00, 960 ^{o}C, O_2 (250 SCCM)	1:56:00, 960 ^{o}C, O_2 (300 SCCM)	1:56:00, 960 ^{o}C, O_2 (300 SCCM)
5	**Lithography**		Done	Done	Done
6	**Silicon Dioxide**		400 nm	400 nm	400 nm
7	**Back-Contact**		-	-	Ti (300 nm)/Au (200 nm)
8	**Lift-Off**		2:00:00	10:30:00	1:00:00
9	**Re-annealing**		1:56:00, 960 ^{o}C, O_2 (250 SCCM)	1:56:00, 960 ^{o}C, O_2 (300 SCCM)	1:56:00, 960 ^{o}C, O_2 (300 SCCM)
10	**LSMO Deposition**	**Thickness**	45 nm	6 nm	9 nm
		Laser Fluency	1.8 J/cm^2	1.8 J/cm^2	2 J/cm^2
		Target-to-Substrate Distance	40 mm	40 mm	40 mm
		Deposition-O_2 Pressure	0.35 mBar	0.35 mBar	0.35 mBar
		Post-annealing	Natural Cooling	Natural Cooling	1:00:00 Plus Natural Cooling
		Post-annealing O_2 Pressure	100 mbar	100 mbar	100 mbar

I-V characteristics of the diodes have been studied using two different systems; one is the conventional probe station where a Keithley meter is used to sweep the applied voltage and the current is recorded using two metallic probes touching the sample surface. The second is the BEEM set up, where the sample is loaded in the BEEM sample holder and the top contact is made using a thin Au metal foil, while the bottom contact is the standard contact used for all BEEM measurements and described both in Chapter 2 and Chapter 6. A schematic representation of such measurement geometry is given in Figure 5.14.

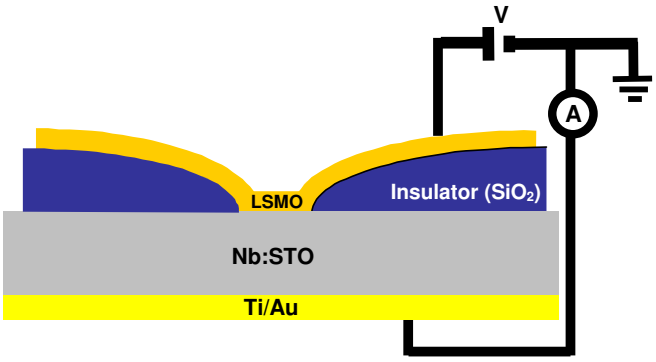

Figure 5.14 a schematic representation of the geometry in which the rectifying behavior of LSMO/Nb:STO junction has been studied.

5.8.1 Diode 1

The I-V characteristics of Diode 1 (Table 5.3) are discussed first. Room Temperature (RT) and low temperature measurements of Diode 1 are shown in Figure 5.15. Negative voltage means that the semiconductor has a negative bias and electrons flow from Nb:STO to LSMO. In the forward bias of the diode, up to 1 V, the forward current is hugely limited by some series resistance and is practically close to zero both at RT and at 100 K. The reverse bias (leakage) current in the diode is a few nA at RT which decreases, as expected, with the lowering of temperature and at 100 K it is ~10^{-11} A at -1 V. No rectification property of the diode is visible. The huge series resistance in the forward direction is quite perplexing but seems to arise from a poorly conducting top LSMO layer, quite contrary to what is seen in Figure 5.13 and therefore poor contact to the metal probes. This further worsens with cooling as LSMO undergoes a temperature dependent resistivity change at low temperature. Such a diode is practically useless and was not used for BEEM studies.

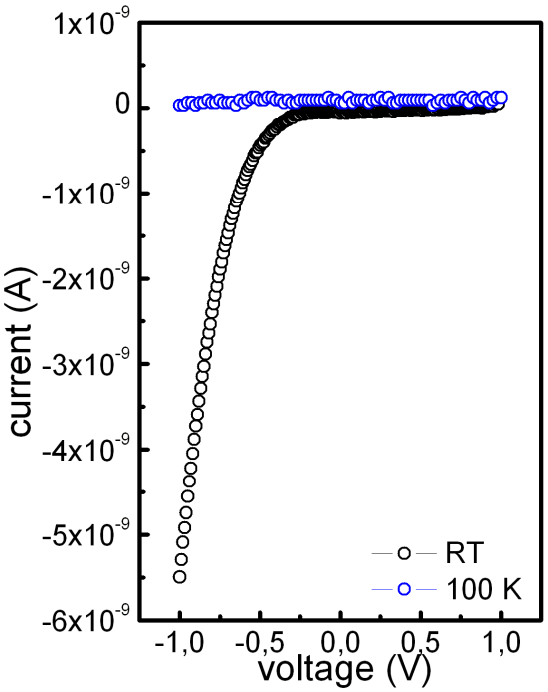

Figure 5.15 I-V characteristics of Diode 1 both at RT and 100 K. At forward bias up to 1 V, the current is negligible. In reverse bias at -1 V, a huge leakage is seen for the diode in RT, while the current is limited to ~10^{-11} A at 100 K.

5.8.2 Diode 2

Diode 2 was fabricated with the conditions mentioned in Table 5.3. As can be seen, a main difference between Diode 1 and Diode 2 is the doping concentration of the substrates (0.01 wt% and 0.05 wt% niobium concentration, respectively) as well as thickness of the deposited LSMO layer (45 nm and 6 nm, respectively). RT I-V measurements were done on this sample and the results shown in Figure 5.16. For this diode the I-V characteristics does show an exponential behavior at low bias and leakage currents at reverse bias conditions of the diode is of the order of a few μA. This raised some prospects for pursuing LT I-V and BEEM measurements with this diode. However, while going to LT conditions, in the 2-probe measurement set up, so as to measure the diode characteristics, we noticed that the diode broke down dashing our hopes of measuring any BEEM transmission in this diode. Although it was bad news, we continued with intense vigor further device fabrication and the results of that will be presented in the next section.

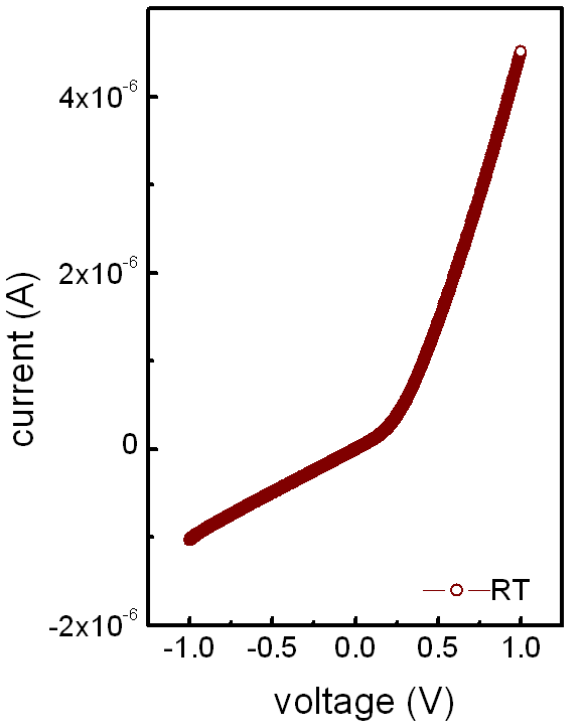

Figure 5.16 I-V characteristics of Diode 2 at RT. A rectifying behavior is seen, however it is not showing the expected diodic behavior. Note that in all negative biases a leakage current exists.

5.8.3 Diode 3

From Table 5.3, we see that Diode 3 differs from Diodes 1 and 2 in quite a few aspects. The first noticeable difference is the thicker back contact that ensures the ohmic nature of the contact throughout the fabrication process and the processing sequence in which such a back contact was made. Secondly, a lower laser fluence (~1.8 J/cm^2) has been used to deposit the LSMO layer as compared to that of Diode 1 and 2 (~2 J/cm^2). The third major difference is the introduction of a new step viz. post-annealing of the deposited LSMO layer. In this step the deposited LSMO film was *in-situ* annealed for one hour immediately after its deposition.

Figure 5.17 (a) shows the probe-station I-V characteristics of Diode 3 at RT (~300 K) and at 250 K. The measurements were done also at 100 K with little change to the I-V characteristics as compared to 250 K. The thickness of LSMO layer in this diode is 9 nm and the STO substrate was doped with 0.1 wt% niobium. At both RT and 250 K, I-V curves in Figure 5.17 (a) shows a regime in the forward characteristics in which the current increases exponentially with voltage. The series resistance limits the current flow beyond a certain voltage which is different for RT and LT. A satisfactory rectifying behavior is observed at both temperatures with a reverse bias leakage of a few pAs. We also see that at 250 K, the onset of current flow is delayed. This is most likely due to mobile charge trapping centres, very often found in such oxide systems. From the exponential part of the I-V curve, we fit the data with the thermionic emission theory [13] as below:

$$J = A^{*}T^{2}\exp(-\frac{q\phi_b}{kT})[\exp(\frac{qV}{nkT}-1)] \qquad 5.3$$

In which ϕ_b is the Schottky barrier height (SBH), n is the ideality factor and A* is the Richardson constant which is 156 $Acm^{-2}K^{-2}$ in the case of STO. If a good fit is found giving n=1, then this indicates that the thermionic emission model fairly well explains the current transport through the diode. In that case, the above fit, will give a correct SBH. However, other transport mechanisms can also be effective, such as direct tunneling, thermally assisted tunneling etc. all of which can make the diodes non-ideal thus influencing the SBH of the diodes.

In our case, using the above equation, the Schottky barrier heights (SBH) of the diode at RT and at 250 K were respectively 1±0.1 eV and 0.85±0.1 eV with n=1.2. Such a temperature dependent SBH has been reported in two earlier works on a similar system and is ascribed to the modulation of the barrier width and permittivity changes of the STO layer [25] [21]. Further discussions will follow in Chapter 6. I-V measurements on the same diode were also done using BEEM system. Figure 5.17 (b) shows such a measurement at 100 K. The absolute value of the reverse bias leakage at -1 V is ~0.3 nA. The current is found to rise exponentially with bias in the forward direction of the diode.

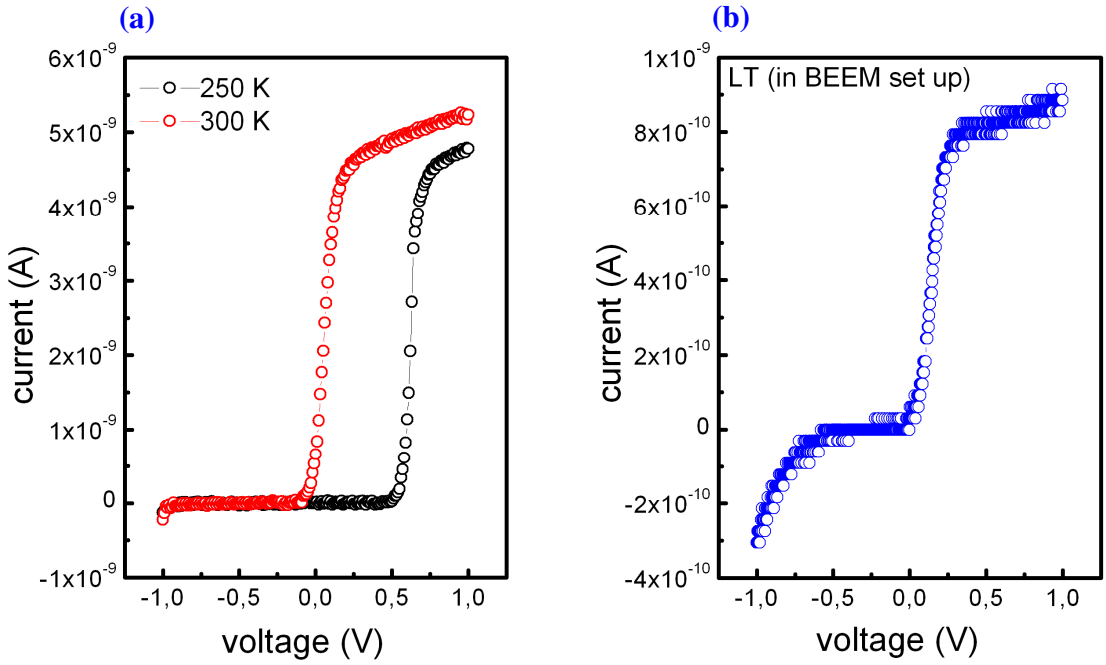

Figure 5.17 LSMO/Nb:STO junction a) probe station measurements at two temperatures. At both temperatures a good rectifying behavior exists. By decreasing temperature, the starting point of current flow in the forward bias shifts to the right. b) LT (100 K) I-V curves obtained from BEEM system. The leakage at -1 V is ~0.3 nA, while at 1 V an already saturated current of ~0.8 nA is measured.

While repeating the measurement for different conditions (of temperature ramping and external magnetic field), it was tempting to increase the applied voltage to the diode. This was done up to a bias of ±2 V, carefully increasing in steps from ±1V. Interestingly, we saw a second sharp onset of current rapidly rising, exponentially, with increasing bias. This has been shown in Figure 5.18 with red arrows. Whereas the first onset is roughly around 0.8 V, the second arises at roughly 1.5 V. It is unclear at this point if one can use the thermionic emission model to determine the SBH of such diode characteristics. Further insight is needed to understand these characteristics.

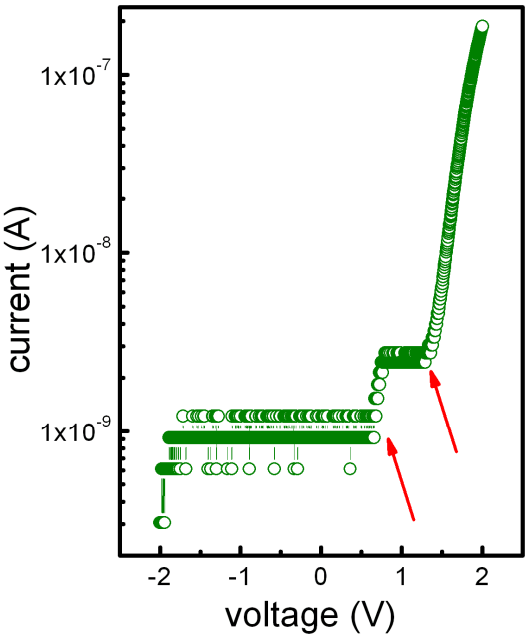

Figure 5.18 LSMO/Nb:STO junction rectifying behavior at LT in a logarithmic scale obtained from BEEM system. Red arrows indicate two onsets in the graph.

5.8.4 Discussion

From the above sections, it is clear that we have successfully fabricated and analyzed LSMO/Nb:STO diodes both at RT and at LT. Diode 3 is the most promising as it has shown a robust behavior with temperature and applied bias and also better rectifying characteristics. Diode 3 happens to be the most intriguing as well. Two onsets of current at two distinct applied voltage might point to the fact that there are several phases existing in the LSMO/Nb:STO diode or that there are several charge traps or localized states in the LSMO layer [26] [13]. The two different SBs act as two parallel diodes. When the applied forward bias is small, the diode with lower barrier height starts to function, with increasing applied bias, the second diode starts to operate leading to two different onsets. Further studies are needed to reproduce and/or understand the origin of such distinctly different phases in such diodes. In the next chapter, we will show the

results of electron transport at such interface (Diode 3), done for the first time, at the nanoscale, using the technique of BEEM.

Chapter 7: Conclusion and Future Perspective

This thesis describes the realization of successful epitaxial diodes of half metallic ferromagnets with Nb doped STO substrate and the observation, for the first time, of hot electron transmission across such an interface. A key feature of any electronic device is the Schottky barrier at the Metal/Semiconductor interface. Replacing the metal with a half-metal having 100% spin polarized carriers could lead to effective spin filtering across a suitable oxide semiconducting interface and lead to the design and operation of novel all-oxide spintronics devices.

After a brief introduction to oxide spintronics in Chapter 1, the various techniques used in this work were described in Chapters 2 and 3 with a special emphasis on the technique and working principle of the BEEM. Since not much is known about the electrical characteristics of the single crystal oxide semiconducting substrates, which widely vary from one supplier to another, a major thrust in this thesis was on understanding the transport mechanisms in Nb-doped STO semiconducting substrates purchased for this work. Chapter 4 discusses the results obtained on two different Nb doped substrates with respect to their carrier concentration, mobility and resistivity. The trends obtained by us match closely with those of published work on similar substrates. In Chapter 5, a detailed account of the fabrication and characterization of the LSMO/Nb:STO diodes has been presented. Fabrication of epitaxial oxide diodes between LSMO/Nb:STO proved quite challenging. By a dedicated work protocol, it was finally possible to realize successful diodes with good rectifying properties. The forward I-V characteristics of one of the diodes show an exponential dependence of the current with voltage using two independent techniques. The exponential part of the forward I-V characteristic could be fitted with the expression for thermionic emission current density in a Schottky barrier. The diode characteristics show very interesting features, never reported earlier. Two onsets of the exponential behavior were observed, one corresponding to 0.8 eV and the other to around 2 eV. The latter was not fitted with the thermionic emission theory and further understanding is needed to understand the appropriate model to be used in such cases. Two onsets of current at two distinct applied voltages might point to the fact that there are several phases existing in the LSMO/Nb:STO diode or that there are several charge traps or localized states in the LSMO layer. Further work is needed to establish or refute this proposition. The most interesting part of this thesis is the observation of hot electron transmission across an epitaxial interface of a half metal as LSMO and oxide semiconducting substrates as Nb:STO. This has been discussed in Chapter 6. Here BEEM was used to study hot electron transmission and its energy dependence, across such epitaxial interfaces at the nanoscale. Two distinctly different regions have been observed in our BEEM studies; one with low Schottky barrier height and high transmission and the other with higher Schottky barrier height and low BEEM transmission. Whereas the lower Schottky barrier height is thought to arise from the epitaxial LSMO/Nb:STO interface and the large transmission is attributed in this case to the epitaxial interface with

reduced momentum scattering, the origin of the higher Schottky barrier height can only be speculated at this point. It might occur from charge trapping centers situated close to the LSMO/Nb:STO interface or could arise from different regions which are electronically phase-segregated. Further, features are observed in the BEEM spectra as changes in the slope of the electron transmission which can be correlated to different reasons such as DOS features in the LSMO or opening up of different energy channels in the semiconducting substrate.

Further work is currently underway to investigate and understand further such epitaxial interfaces and the rich physics of these complex oxides at higher energies. This work is a first step forward and is expected to open up new horizons in half-metals and other complex oxides relevant to the emerging field of Oxide Spintronics.

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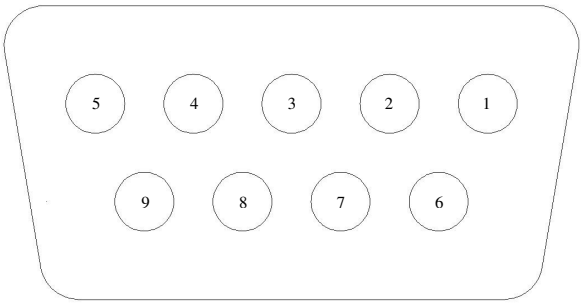
Appendix I: BEEM's Cooling System Control

Nine-pin connector that links the ITC503 temperature controller to the sensor and heater inside the cryo is numbered as follows:



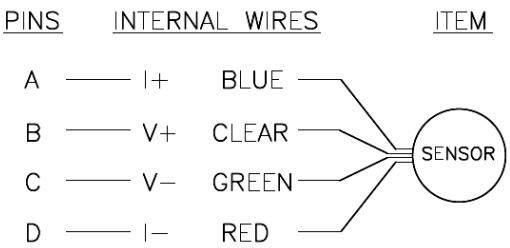
In this pin-connector :

1- Input High
2- Input low for Normal Applications
3- Input GND (Linked to pin 2, isolated from supply GND)
4- Current Source +ve
5- Current Source -ve
6- Heater Output +ve
7- Heater Output -ve
8- Input Low for Thermocouples with RT Ref. Junction
9- Chassis Ground

Connections between this socket and the actual sensor will vary with the type of sensor in use, as shown in the table below:

	Thermo-couple	Metal Resistor	Ge/Carbon Resistor	Si/GaAs Diode
Input High	V+	V+	V-	V-
Input Low	V-	V-	V+	V+
Current +ve	n/c	I+	I+	I+
Current –ve	n/c	I-	I-	I-

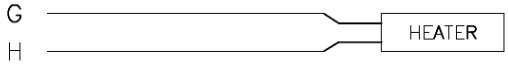
The in-built cryo sensor in our BEEM system is a Silicon diode that can measure from 1.5 K up to 475 K. This sensor requires a wiring to the controller based on the right column of the above table. Moreover, the connections to the sensor and the heater are schematically shown in next figure:



SENSOR INFORMATION

TYPE:	SILICON DIODE
MODEL NO.:	DT−670B−SD
SERIAL NO.:	D6010935
CURVE NO.:	LS−11
LOCATION:	SAMPLE MOUNT

E	I+	BLUE
F	V+	CLEAR
J	V−	GREEN
K	I−	RED



HEATER INFORMATION

TYPE:	FILM
RESISTANCE:	25 OHM
LOCATION:	SAMPLE MOUNT

Appendix II: Image Reversal TI35ES Photoresist

In an image-reversal lithography mode, resist attains negative sidewalls. This undercut geometry minimizes the coverage of the coated films onto the resist sidewalls and thus makes the lift-off process much easier compared to positive resists. Image reversal resists can be processed in either positive or negative modes. The steps followed in our device preparation are listed here:

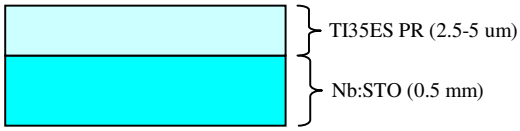
1. **Prebaking for 10 min at 120 °C**

   To make sure that the water has evaporated completely from the substrate.

2. **HMDS spin coating for 20 seconds in 4000 RPM**

   Used for better adhesion of photoresist.

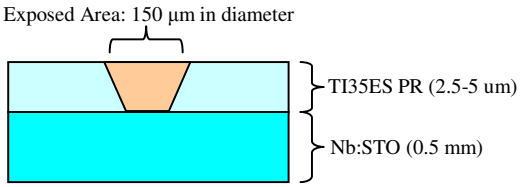
3. **TI35ES spin coating for 20 seconds in 4000 RPM**



4. **Soft baking for 2 minutes at 95 ^{o}C**

5. **24 second exposure to UV light**

   Exposure of the resist part which later should not be developed.

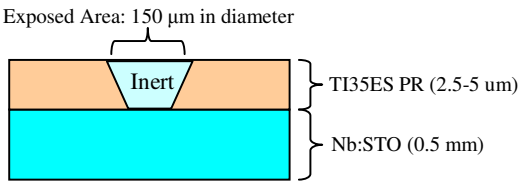


6. **Degassing for 45 minutes at room temperature**

   Prevents formation of nitrogen bubbles in the resist.

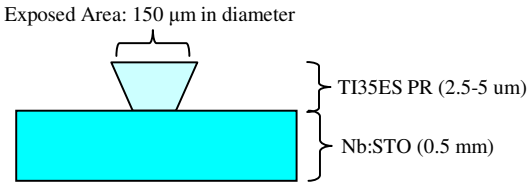
7. **Image reversal baking for 2 minutes in 120 ^{o}C**

   This step makes the exposed area insoluble in developer.



8. **Flood exposure for 60 seconds using UV light** Makes the so far unexposed resist, developable.

9. **Development for 45 seconds using OPD-4262**



10. **DI rinsing**

11. **Spin dry**