Taking topological insulators for a spin

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Chapter 3

Studying charge transport at metal/topological insulator interfaces

Topological insulators host interesting properties for many applications in physics and its implementation in solid-state device geometries necessitates studying charge transport at the interface between a topological insulator and other materials. Theoretically and experimentally, it has been observed that metals in the proximity of topological insulators give rise to potential variations, which can be crucial for preservation of the topological surface states and the transport across the interface. By performing three-terminal measurements in solid-state device geometries as well as employing measurement techniques involving hot charge carriers, we have studied charge transport across these metal/topological insulator interfaces at different lateral scales in order to gain more insight into the electrostatic landscape of such interfaces. From the experiments, we do not observe a consistent presence of a (Schottky) barrier at the interface, which is in line with theoretical works that studied metal/topological insulator interfaces. The apparent presence of a barrier in several cases can be related to the likely presence of contamination layers, originating from the device fabrication procedure. Furthermore, artifacts related to one of the employed measurement setups has caused the spurious appearance of a barrier. Definitive conclusions on the presence of a barrier cannot be made due to the low yield of devices; future experiments have to shed light on this.
3.1 Introduction

The special properties of topological insulators as theoretically proposed and shown experimentally pave the way towards new solid-state device geometries (see chapter 7). Implementation of these materials in such geometries necessitates studying electrostatics-related phenomena at the interface with other material systems for two main reasons. First, since these materials can be considered small band gap semiconductors, interfacing topological insulators with metals could obviously lead to Schottky barriers. The presence of such a barrier limits the efficiency of charge or spin injection and extraction in device geometries. Understanding the origin of such a barrier can lead to low-dissipation applications. Furthermore, potential variations at the surface can give rise to additional 2D confined states that are spin textured. These topologically trivial states have an opposite net spin texture compared to the topologically nontrivial states and therefore can suppress the generated spin accumulation in the topologically protected surface states. This potentially could yield a lowering in the efficiency to use topological insulators for spintronic applications.

Variations in electrostatic potential at the surface of a topological insulator can be related to Fermi-level-mediated differences in charge-carrier density between bulk and surface [1–4]. The degree of bending depends on the relative Fermi levels at the surface and the bulk where the bulk Fermi level is often bound to the conduction band edge [3]. From the bulk Fermi level, it is then possible to calculate the surface-state charge-carrier density $n_{SS,FB}$ for the flat-band condition. Downward bending occurs for $n_{SS} > n_{SS,FB}$, and upward bending takes place in the case of $n_{SS} < n_{SS,FB}$. One obvious method to tune the degree of bending is application of an electrostatic gate in which the Fermi level is tuned and thus the charge-carrier densities of the respective channels. Gating of topological insulators has been realized by many groups in which the top and bottom surface can be independently controlled [10–22]. This independent control can be ascribed to the large dielectric constant of around 100 found for this class of materials [23,24], which gives rise to an efficient screening of the electric field into the bulk. Therefore, gating to suppress the bulk charge-carrier concentration is limited and will lead to intermixing with surface-state transport. In order to reduce bulk contributions, one has to look into alternative growth techniques that reduce or compensate the defect density and thus the bulk conductivity (see section 2.4).

In addition to gating, band bending can be caused by the presence of organic adsorbates or residues [6,25–34]², due to bonding or elemental reconstructions in the crystal structure [4,8,37–40], due to an incident high flux photon beam [33,41–44]³, and can be modified by interfacing the material with (magnetic) metallic or molecular layers [5,7,15,26,45–58]. In many of these works involving ARPES, it has been observed that additional 2D states with an opposite spin texture exist, which is more difficult to probe in a charge-transport measurement.

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¹One important consequence of this picture is that by reducing the thickness of films that show an upward bending and have no impurity bands, it is possible to deplete the full bulk layer. This can lead to full surface-dominated transport [5], especially in connection to experimental works that report that this bending can extend up to 20 nm into the bulk and thus could be experimentally easily realized [6–9]. Nevertheless, usually downward bending is reported.

²Although other works report differently [35,36].

³High flux photon beams can change the outcome of an ARPES experiment.
Introduction

From most of these ARPES studies, it has been shown that downward bending occurs at the surface of Bi₂Se₃. The electron affinity and the work function of Bi₂Se₃ are known to be 5.3 eV [59] and 5.7 eV [60] respectively, where the work function was experimentally found to be 5.6 eV [61]. These values are larger than the work functions of common metals which are usually below 5 eV [62]. Intuitively, it is thus expected that electron transfer occurs and thus an accumulation-type Schottky barrier with downward bending is present at the interface with a metal [51,59,60]. However, the sole comparison of the semiconductor’s electron affinity and the metal’s work function is an oversimplified picture in reality as interface effects are to be included [64]. As an example for the case of topological insulators, it has been calculated that even for high work function metals such as Pt (work function of 5.6 eV) similar potential landscapes as those for metals with lower work functions occur due to the large electronegativity of the top Se layer. Additionally, it has been proposed in the aforementioned works and other works [50,65,66] that wave functions of metals can overlap with those of the topological insulator, which leads to hybridization. This will strongly suppress charge transport through the spin-textured surface states only. Even if the coupling between metal layer and topological insulator is weak upon imposing a separation of a few Å, the electronic structure will still be affected which is especially the case for magnetic metals. The strong modulation of the topological surface states by normal metals’ electronic states adds to the possibility to change the surface states by breaking time-reversal symmetry microscopically. Breaking this symmetry can be for example done by magnetically doping the topological insulator [14,67–69] or by interfacing it with a magnetic layer [70–77], which depends on the orientation of the magnetic moments at the interface [49,50,58,78]. As discussed by Zhang et al. [60], these effects could have implications for spin-torque and magnetization switching measurements. As proposed for future spintronic devices, a tunnel barrier is required in order to remove the direct interaction between metal and topological insulator [59].

The above considerations indicate that Ohmic interfaces between topological insulators and the majority of metals exist. Nevertheless, Ye et al. investigated transport across interfaces between transition metals and Bi₂Se₃ where W tips coated with Cr, Ni, or Co were brought into contact with the topological insulator [79]. From two-terminal measurements, it was found that a barrier seems to be present. However, the yield of working devices was low and additional analysis on the possible Schottky barriers was lacking. For junctions with Ni and Co, the I–V characteristics seem to indicate that an oxidation or contamination layer was present, resulting in a low barrier height that becomes transparent at moderate voltages rather than a real Schottky barrier with rectifying properties. For the case of Cr, a low rectification of 2.6 at

\footnote{This type of barrier can be visualized as the forward-bias-regime picture beyond the flat band condition in a Schottky barrier. In this picture, a lot of electrons are present in the otherwise charge-depleted region allowing efficient charge transport across an Ohmic barrier. It has to be noted that the semiconductor’s degeneracy, which is the difference between electron affinity (energy between conduction band minimum and the vacuum level) and the work function (energy between Fermi level and the vacuum level), is included in the built-in potential that majority carriers have to overcome to reach the metal [63]. In charge-transport models considering Schottky barriers as in thermionic emission, the degeneracy does not play a role because in the expression for the current this parameter appears twice and cancels out. Therefore, details on the electron affinity are more valuable, which can be deduced from the work function once the Fermi level is known.}
a bias of $\pm 0.4$ V was visible, which suggests the presence of a low Schottky barrier. However, a clear exponential behavior was missing, which could be masked by a series resistance coming from Bi$_2$Se$_3$. Temperature-dependent studies and analysis of the $I$–$V$ characteristics are crucial to make definite conclusions on the presented results.

An alternative geometry to avoid direct coupling between metal and topological insulator is proposed by Ojeda–Aristizabal et al. [80]. Here, the (ferromagnetic) contact is separated from the topological insulator by a thick Si layer, which surprisingly leads to Schottky barrier formation at the Si/Bi$_2$Se$_3$ interface where its barrier height has been derived from the ionization potential for Bi$_2$Se$_3$ of 4.45 eV. Notably, the use of the term ‘ionization potential’ in the paper is unclear since this concept refers to ionization of independent atoms and is unrelated to the electron affinity or work function of an alloy. Furthermore, if the value of 4.45 eV would correspond to either electron affinity or work function, this value is low compared to the values cited earlier in this section, which could suggest that heavy modification at the surface of Bi$_2$Se$_3$ has caused the observed Schottky-barrier-like behavior. Essential information is missing in order to make conclusive statements about this report.

Although the literature on this topic has by now clarified some open questions from the aforementioned works, we have performed experiments in an early stage of this project based on the quoted value of the presumed affinity of 4.45 eV. Therefore, we have used metals with a high work function such as Pt so as to create a Schottky interface as well as metals with a lower work function for reference. The charge transport at such an interface has been studied by means of three-terminal solid-state devices, in a hot-electron transistor scheme, and by employing the measurement scheme of ballistic-electron emission spectroscopy. From these experiments, we do not observe clear signatures of the presence of a barrier at the interface, which would be in line with theoretical propositions and experimental work. However, the absence could be partially due to technological difficulties encountered.

### 3.2 Measurement schemes to study transport at the interface

This section deals with the various measurement schemes that have been used in order to study metal/topological insulator interfaces. Here, we assume that the topological insulator Bi$_2$Se$_3$ acts as an $n$-type semiconductor such that an Schottky barrier is formed, based on the values reported by Ojeda–Aristizabal et al. [80]. In the first part, theoretical concepts regarding the measurement schemes will be briefly presented. In the second part, details on the device fabrication of these geometries will be discussed.

#### 3.2.1 Ballistic-electron emission microscopy

Ballistic-electron emission microscopy (BEEM) is a powerful technique used for investigation of buried interfaces and is based on STM for which the measurement scheme can be found in figure 3.1a. In STM, a metal tip injects nonequilibrium ‘hot’ carriers into a conducting ‘base’ layer via the tunneling mechanism. This mechanism allows to probe local variations in the (un)occupied density of states of the base material and it
Measurement schemes to study transport at the interface

Figure 3.1: (a) Measurement scheme of BEEM. Here, the collector substrate is displayed in gray, the thin base layer in orange, and the STM contact pad in dark yellow. An STM tip injects electrons dictated by tunneling current $I_T$ and tunneling voltage $V_T$. Electrons surpassing the base/collector interface are collected at $I_B$. (b) Alternative BEEM geometry in case the substrate (gray) is an insulator (sapphire) and Bi$_2$Se$_3$ is grown on top (green). Here, a collector contact is designed on the Bi$_2$Se$_3$ layer (large pad in yellow) to collect the BEEM current $I_B$ that is coming from surpassing at the metal/topological insulator interface on the right. (c) Corresponding energy band diagram for the BEEM measurement scheme with color coding as in (b). Edited from [83].

gives nanoscale resolution in all dimensions around the surface of the film. Tunneling yields a momentum-filtered hot-electron current $I_T$ with energies $E \gg E_F$ that is injected into the base where $E$ is tuned by the tunneling voltage $V_T$ (figure 3.1c). Depending on the unoccupied density of states in the base, an energy distribution of the electron is formed, peaking close to $E_F - V_T$ [81, 82]. These hot electrons traverse through the entire thickness of the base layer where they can probe the interface between buried layers, and is only possible when the hot-electron lifetime in the base is long enough. This probability can be found from the product of the group velocity and hot-electron attenuation length and depends on $E$ relative to $E_F$ [63].

Depending on the height of the interface barrier relative to the energy of the hot electrons and their angle of incidence (also energy-dependent), these electrons either surpass the barrier or are scattered into the base. In the case of traversing the barrier, the electrons can be collected in the collector layer and the resulting current is referred to as the BEEM current, $I_B$. In a typical measurement, $I_B$ is recorded as a function of $V_T$, which is expected to show an onset when $V_T$ is large enough to surpass the energy barrier. Such a barrier is assumed to be a Schottky barrier in the context of this chapter. This onset is thus a measure for the barrier height $\phi_B$ and can be described by the Bell–Kaiser theory. This theory takes into account conservation of energy and transversal momentum, assumes a free-electron dispersion relation for tip and base, and assumes a parabolic dispersion for the semiconductor collector. Close
to the threshold, this theory predicts [84]:

\[ I_B \propto I_T (V_T - \phi_B)^2, \]  

(3.1)

from which we can extract \( \phi_B \).\(^5\) Besides determination of \( \phi_B \), the BEEM transmission \( I_B/I_T \) contains information on the hot-electron scattering in the base. Very often, the shape of \( I_B/I_T \) can provide qualitative information on the type of scattering in addition to being sensitive to any features in the density of states at high energies. One important requirement to have a proper BEEM operation is that the backflow of charge carriers from collector into the base is limited, such that there is a measurable \( I_B \). This backflow of charge carriers is measured as the leakage current at zero bias. A reduced leakage current can be conveniently realized by having a proper barrier resistance such that current fluctuations as a result of fluctuations in the potential are suppressed \[82\]. Besides electrical shielding of the setup to prevent pickup noise, having a Schottky barrier with a considerable rectification will reduce the leakage current. Depending on the barrier properties, low background levels can be obtained and can be further tailored by reducing the device area or temperature.

Compared to standard three-terminal measurements to investigate barrier properties at the interface (section 3.2.3) where the voltage drops over the barrier, the scheme of BEEM allows one to probe such barriers without a created potential difference over the barrier and is thus an efficient tool to probe the pristine barrier across an interface. The investigation of such pristine barriers is possible due to the ‘remotely’ produced out-of-equilibrium hot-electron distribution created by the STM tip. Another advantage of BEEM over three-terminal measurements is that a high lateral resolution is obtained, such that nanoscale variations in the barrier properties can be detected. Furthermore, hot-hole microscopy and spin-selective spectroscopy using ferromagnetic layers can be performed, making BEEM a versatile system to probe buried and pristine interfaces with different electronic density of states. For topological insulators specifically, hot-electron spectroscopy can be a very suitable technique for studying the unoccupied states. Here, a second topological surface state has been observed \( \sim 1.5 \) eV above the band gap \[86–88\], which can potentially contribute to the spin dynamics of hot electrons \[89\].

\(3.2.2\) Hot-electron transistor

The scheme of the hot-electron transistor (HET) can be regarded as a solid-state device realization of the BEEM geometry where buried interfaces can be probed upon injection of a hot-electron distribution. Instead of an STM tip spatially separated from the base by a vacuum barrier, a metal/insulator or metal/semiconductor structure (yielding a Schottky barrier) is employed as hot-electron emitter in such a transistor \[63, 81, 90\]. In contrast to the usual in-plane orientation used in a field-effect transistor, HET schemes are based on a perpendicular-to-plane picture where the base current controls the transmission through the transistor rather than the current fluctuations as a result of fluctuations in the potential.

\(^5\)The quadratic dependence can deviate due to scattering effects in the semiconductor and quantum mechanical reflection \[85\]. This can lead to an exponent of 2.5 as described by the Ludeke–Prietsch model. Differences in the exponent are difficult to observe since these models only apply close to the threshold of \( I_B \), within 0.2 to 0.3 V \[82\].
gate voltage [91]. Nevertheless, this structure has been mainly used for fundamental studies on hot-electron characteristics in various metals, probing the unoccupied states [92–95]. Technological applications based on HET are scarce (yet) because of its limitations of operation at high frequencies, current density and area limitations, and limited gain [81,93].

The operation and type of measurements are very similar to the scheme of BEEM where usually the emitter current \( I_E \) (instead of \( I_T \)) and the collector current \( I_C \) (instead of \( I_B \)) are quoted. From the same Bell–Kaiser theory as used for analysis of BEEM spectra, the barrier height \( \phi_B \) can be extracted, while the gain \( \alpha = I_C/I_E \) yields information on the scattering in the base. In contrast to BEEM where \( I_T \) is set constant, the collector current \( I_C \) will be largely displaying the tunneling characteristics of the emitter given by \( I_E \). The gain \( \alpha \) therefore provides more details on the actual hot-electron characteristics.

### 3.2.3 Three-terminal measurements

Three-terminal measurements have been a convenient tool for exploring interface effects in various fields of solid-state physics. In this geometry, a current is sourced using two contacts located on the conducting channel where one contact is shared with the voltage probe that has a reference to a third contact; a schematic of this geometry can be found in figure 3.2a. Because of the properties of a voltage probe \( (R_{\text{in}} \rightarrow \infty) \), no current is flowing through this part of the device and therefore only the voltage drop over the interface of interest and corresponding lead resistances is measured, as indicated in the figure by \( R_{\text{C2}} \). This allows to measure charge-transport characteristics of solely the interface, provided that the series resistance due to leads, filters, etc. does not play a dominant role. The scheme as depicted has one disadvantage in that the source could force a current through the junction, which can be dangerous for high impedance systems since large potentials can yield damage to the device. In an alternative setting of the source, a two-terminal voltage \( V_{2T} \) is sourced and a two-terminal current is probed where an additional voltage probe \( V_{4T} \) acts as a feedback to the voltage source in such a way that we can control the voltage sourced over \( R_{\text{C2}} \) (figure 3.2b). This can be realized by using the four-wire-sensing mode in the Keithley 2410 multimeter.

![Figure 3.2: (a) Three-terminal geometry with contact resistances \( R_{\text{C1}}, R_{\text{C2}}, \) and \( R_{\text{C3}} \) and channel resistances \( R_{\text{Ch1}} \) and \( R_{\text{Ch2}} \). A current is sourced on the left-hand-side circuit and the voltage is effectively measured over \( R_{\text{C2}} \). (b) Alternative three-terminal geometry where a 2-wire voltage \( V_{2T} \) is sourced in such a way that the desired voltage \( V_{4T} \) drops over \( R_{\text{C2}} \). The resulting current through this junction is measured by the ammeter.](image)
Various charge-transport mechanisms across the metal/topological insulator interface, which we assume to be characterized by a Schottky barrier, can come into play. This depends on the specific electronic characteristics of the system and can be usually disentangled by temperature-dependent studies. A brief overview of these mechanisms can be found in the thesis by Kamerbeek [96].

3.3 Device fabrication

In this section, the fabrication recipes for devices to study charge transport at the interface between metal and topological insulator are briefly described. More details can be found in the appendix at the end of this thesis. The project started out with the realization of BEEM devices (section 3.3.1). Thereafter, we studied transport phenomena in solid-state device schemes (three-terminal geometry and HET) of which the fabrication will be discussed in section 3.3.2.

3.3.1 BEEM devices

In conventional BEEM devices, the collector contact is fabricated on the backside of the semiconductor [83, 97]. However, in the case of studying metal/topological insulator interfaces there is the problem that the collector layer of topological insulator material is grown on an insulating sapphire substrate such that a back contact cannot be realized. Efforts by Roy [98] have led to an alternative scheme where the Ohmic collector contact is realized on top of the semiconductor next to the injector contact. The adjusted scheme is shown in figure 3.1b and will be used for investigation of the metal/topological insulator interface in this chapter.

We have utilized MBE-grown Bi$_2$Se$_3$ on sapphire from which we realized devices by a combination of UV lithography and electron-beam evaporation steps as described by Burema [99]. The devices consist of a Bi$_2$Se$_3$ film on which a series of large Au(10 nm)$^6$ or Pt(4) pads is fabricated, which will serve as the base. The chosen thicknesses are based on the different attenuation lengths, which differ a factor of 4 for Au and Pt [63]. These two materials are selected based on their work function relative to the quoted work function of 4.45 eV [80], where Pt is expected to form a clear Schottky barrier and Au a rather low or no barrier [62]. Inside or connected to these pads, thick contact pads have been fabricated consisting of the base material such as to avoid introduction of other interfaces. The device has been finalized by a large-area collector contact pad next to the fabricated junctions consisting of Ti(5)/Au(70). The large area of the pad and having Ti at the interface for its relatively low work function and good adhesion are chosen in order to maximize the Ohmic character of the contact. Two examples of the final devices are depicted in figure 3.3 in which the base layers are hardly visible because of the small thickness. Furthermore, an atomic force microscopy (AFM) image is shown for the Pt(4)/Bi$_2$Se$_3$ in figure 3.3c, which shows a root mean square (RMS) roughness of 8 Å over the complete image. Triangular patterns as usually observed for Bi$_2$Se$_3$ are still visible after deposition as indicated by the yellow arrow in figure 3.3c. This feature can be compared to

\[ \text{For the remainder of the thesis, the unit is nm unless otherwise mentioned.} \]
Device fabrication

that displayed in figure 3.3d, where a RMS roughness of 6 Å over the same area as for figure 3.3c was found. For the first measurements, the samples as shown in figure 3.3a and 3.3b were clamped on the sample holder by a sapphire washer. This washer contains a spring contact that forms a connection between the STM contact close to the base and to the sample holder body (ground) via one of the clamps. The collector contact was connected through a silver-pasted copper wire to the external BEEM contact on the sample holder.

The measurements have been performed in a commercial RHK-UHV 300 variable-temperature, ultra-high-vacuum STM of which the details can be found in the theses by predecessors of the group [83,97,98].

Figure 3.3: (a) BEEM device with Au(10) base (inside open red squares) on Bi$_2$Se$_3$ (gray) with a Au(70) contact pad extruding out of the base (inside open blue square) and collector contact on the left. (b) BEEM device with Pt(4) base and inside Pt(76) contacts. Here, the collector contact was designed smaller but this did not influence the device performance. (c) AFM image after deposition of the Pt(4) base on Bi$_2$Se$_3$. The arrow emphasizes the presence of the buried triangular pattern of Bi$_2$Se$_3$. (d) AFM image of the same device outside the contact pattern area that depicts the Bi$_2$Se$_3$ surface. An artifact at the surface is visible.
3.3.2 Solid-state device geometries

Nanometer-sized junction area devices — In order to locally probe the presumably low barrier height with resulting leakage-current issues, nanoscale-sized device geometries have been realized through a new fabrication recipe. Here, small topological insulator strips of 100 and 200 nm are designed from large area Bi$_2$Se$_3$ thin films together with Zillen [100]. These films have been engineered into free-standing strips of 100 and 200 nm in width by defining them with electron-beam lithography (EBL) using a positive PMMA resist. This means that the complete resist layer has to be exposed except the strip lines whereafter the topological insulator material can be largely etched away. In order to do so, we have employed extensive dose testing since proximity effects play an important role in structures where the complete area has to be exposed except for a small protective polymer strip. The ideal dose is found to be between 180 and 225 µC/cm$^2$ (30 kV, 7.5 µm aperture), which is considerably lower than the nominal dose of 450 µC/cm$^2$ usually employed. In order to maintain a clean interface between the metal and the topological insulator, we have created small square metal pads in an early stage of the fabrication. The dose for writing these small structures has been optimized based on the sharpness of the structures. The optimal dose varied between 450 and 630 µC/cm$^2$ where the higher dose factor has been used for the smaller pads. The final dimensions of the pads are 10 to 20% off from those designed beforehand.

For the final device, a large contact pattern and markers have been defined by DUV lithography and electron-beam evaporation of Ti(5)/Au(70) on 20 QL Bi$_2$Se$_3$ films. Thereafter, Pt(30) metal protection pads have been designed by EBL and electron-beam evaporation. Etched patterns are designed by a combination of DUV lithography and EBL lithography and etched by reactive-ion etching. In the last step, Pt(30) contact leads have been defined by EBL and deposited by electron-beam evaporation to account for any misalignment between metal pads and etched topological

![Figure 3.4: (a) Solid-state device with 100 (bottom) and 200 nm (top) Bi$_2$Se$_3$ strips (horizontal) and Pt contact leads (vertical). (b) SEM image of junction on 100 nm wide strip showing that the Bi$_2$Se$_3$ is discontinuous. At the junction the square protection pad is visible.](image-url)
Device fabrication

insulator strip. A picture of the final devices that have been measured is shown in figure 3.4a. As can be seen by the shadows at the contacts, the adhesion of the Pt is not proper everywhere. Furthermore, the 100 nm wide strips are discontinuous as can be seen from SEM images in figure 3.4b. In addition to that, the etching procedure has not been uniform over the whole substrate, the origin of which is unknown. Due to these issues, the yield of well-functioning junctions has been low and only few three-terminal measurements have been performed on junctions with an area of about $200 \times 200 \text{ nm}^2$.

*Three-terminal devices using topological insulator flakes* — Next to these devices, we have fabricated three-terminal devices based on the quaternary compound $\text{Bi}_{2-x}\text{Sb}_x\text{Te}_{3-y}\text{Se}_y$ (BSTS), as introduced in section 2.4. From these materials, it is expected that the surface-state contribution is relatively large, but this is accompanied by a decrease in mobility due to the introduction of Sb and Se in the original $\text{Bi}_2\text{Te}_3$ matrix. These counterdoped compounds have been mechanically cleaved from bulk crystals supplied by the Ando group [101–103]. As reported by Hoogeboom [104], the strong bonding between the quintuple layers requires a higher adhesive tape, which leaves a considerable amount of glue residue that can be removed by immersing the substrate with BSTS flakes into (heated) acetone and isopropanol. The resulting flakes can be observed by optical microscopy up to thicknesses of $\sim 80 \text{ nm}$ since in general the lateral dimensions reduce with reducing thickness. This can be improved by maintaining a small angle between tape and substrate when cleaving. For these experiments, $n$-type $\text{Bi}_{1.5}\text{Sb}_{0.5}\text{Te}_{1.7}\text{Se}_{1.3}$ and $p$-type $\text{Bi}_1\text{Sb}_1\text{Te}_1\text{Se}_2$ were used.

The flakes were exfoliated on heavily $n$-doped Si substrates that have a 300 nm SiO$_2$ layer for gating purposes. In order to study interfaces between BSTS and different metals, multiple EBL and electron-beam evaporation steps were employed in order to deposit different metal contacts on the flake. Since the flakes are of consid-
Studying charge transport at metal/topological insulator interfaces

Considerable thickness, metal contacts were evaporated under a tilt angle while rotating in order to have a proper coverage at the sides of the flake. This procedure increased the yield of working junctions slightly, but it is recommended to determine the flake thickness prior to metal evaporation. In this way, the metal can be made thick enough to make proper contact with the flake. Two examples of such devices are shown in figure 3.5 where the device displayed in figure 3.5b further serves for basic electrical characterization of the flake to extract charge-carrier density, charge-carrier type, and the charge-carrier mobility.

**Hot-electron transistor** — As developed by Burema [105], topological insulator-based hot-electron transistors have been realized using Ca-doped Bi$_2$Se$_3$ samples in which Ca$^{2+}$ atoms are substituting Bi$^{3+}$ atoms and thus act as hole donors [38, 106]. These holes first compensate the excess electrons before the material turns $p$-type. The samples consist of a 5 QL In$_2$Se$_3$:Bi$_2$Se$_3$ (50:50) capped 20 QL Ca-doped Bi$_2$Se$_3$ grown on an insulating buffer layer of 20 QL In$_2$Se$_3$:Bi$_2$Se$_3$ (50:50) to enhance the charge-transport properties (see section 2.4), which is in turn grown on an Al$_2$O$_3$(0001) substrate. These layers are grown by MBE and received from our collaborators from Rutgers University. Performed Hall measurements in a physical property measurement system (PPMS) confirm the $p$-type majority carriers with a charge-carrier density of $\sim 2.5 \times 10^{12} / \text{cm}^2$ at $T = 10, 160 \text{ K}$, which increases to $\sim 4.0 \times 10^{12} / \text{cm}^2$ at $T = 300 \text{ K}$ (see figure 3.6a). This results in a Fermi wavevector $k_F = \sqrt{4 \pi n_{2D}} = 0.06-0.07 \text{ Å}^{-1}$, being close to the Dirac point$^7$. From the residual $\delta = R_{\text{data}} - R_{\text{fit}}$ in the Hall measurements, a second channel seems present. However, a two-carrier model cannot be fitted due to the small contribution of this channel.

From these grown layers, HETs have been fabricated as follows. First, an insulation layer of AlO$_x$(50) having junction holes with diameters ranging from 5 to 150 µm is grown to prevent direct contact between base and collector. Then the base contacts of Au(8) are deposited, whereafter a second insulation layer is grown to prevent direct contact between base and emitter. In the last step, an AlO$_x$(2) layer is grown by two rounds of Al(1) deposition, followed by plasma oxidation and the emitter contact of Au(70). The resulting device is shown in figure 3.6b.

In this geometry, as sketched in the inset of figure 3.6b, it can be seen that there is a chance of having a direct connection between base and emitter since the extent of the tunnel barrier at the side walls is unclear. This probability can in the future be avoided by using the insulation mask sizes in the reverse order such that the emitter contact falls inside the active area at the base. Furthermore, it has to be noted that the insulating 5 QL In$_2$Se$_3$:Bi$_2$Se$_3$ (50:50) capping layer is still present and therefore a direct interface between metal and topological insulator is absent. In this metal-insulator-semiconductor structure, part of the potential due to the depletion layer will fall over the capping layer. The modified band diagram including the capping layer and $p$-type character of the collector is shown in figure 3.6. Rather than employing hot-electron spectroscopy, hot holes will be revealing the barrier characteristics via a very similar working principle.

$^7$However, it is difficult to have hole-like transport from the surface states alone since for Bi$_2$Se$_3$ the Dirac point almost aligns with the valence band maximum [38] and therefore careful control of Ca doping is required.
In this section, the measurement results based on the devices discussed in the previous section will be presented.

3.4.1 BEEM devices

Measurements for the first three devices and fabrication of subsequent devices have been performed together with Burema [99]. The measurements consist of two-terminal
measurements between the STM contact and the BEEM contact to investigate the leakage current and rectification of the barrier at the base/collector interface. Furthermore, BEEM has been attempted but no clear results have been obtained, which will be discussed throughout this section.

The first three devices with Au(10) and Pt(4) metal base layers that were mounted on the holder with a spring contact show nonlinear behavior in the two-terminal $I-V$ characteristics with a very weak rectification ($I_{\text{forward}}/I_{\text{reverse}} \approx 1.3$ at $\pm 0.3$ V) and a leakage current level between $10^{-6}$ and $10^{-8}$ A at room temperature (RT), see figure 3.7a and 3.7b. The absence of a reasonable rectification and the presence of a nonlinear curve suggests the presence of a tunnel barrier. The transport through such a barrier is thermally assisted as observed from the linear slope in addition to the tunneling characteristic. Upon cooling to $\sim 110$ K [indicated by low temperature (LT)], the linear slope as observed at RT disappears and the tunneling characteristic for Au(10)/Bi$_2$Se$_3$ becomes more prominent (figure 3.7a). However, the measured current decreases by several orders of magnitude as well. Furthermore, the leakage current decreases to $10^{-10}$ A, which would yield a good starting point for obtaining BEEM spectra above the leakage current level. For the case of Pt(4)/Bi$_2$Se$_3$ devices (figure 3.7b), the current is below the detection level of $10^{-10}$ to $10^{-11}$ A up to $+1$ V bias, which suggests that either the tunneling performance increases over a longer bias range or that the spring contact connecting the STM pad is now physically separated due to thermal contraction of the contact. The observation of a finite current beyond $+1$ V bias (lower inset figure 3.7b) indicates that the spring contact would be still in close proximity of the STM contact. Unfortunately, the $I-V$ characteristics for both devices have not been measured for larger negative bias to analyze the tunneling behavior or rectification.

The low leakage current levels from the two-terminal measurements at LT give

![Figure 3.7](image-url)
Results and Discussion

confidence of investigating the barrier via the scheme of BEEM, although the presence of a barrier is not clear from the $I-V$ characteristics. The absence of a strong rectification could yield backflow of injected hot electrons from the collector into the base. From the BEEM measurements for device Au(10)/Bi$_2$Se$_3$, we find a background BEEM current $I_B \sim -0.4$ pA with a noise bandwidth of $\sim 0.1$ pA at $I_T = 80$ nA, where the negative sign for $I_B$ indicates that electrons are collected. Compared to the lowest values for $I_B/I_T$ in the alternative geometry on the order of $10^{-4}$ pA/nA [98], the observed background level is 10 times lower and a measurable BEEM response can be expected. However, after taking maximally 200 BEEM spectra up to 2 V with respect to the Fermi level and by taking its average, we do not find any clear onset outside the noise bandwidth in $I_B$ that could signify surpassing of a Schottky barrier. Similarly for Pt(4)/Bi$_2$Se$_3$, although we find a lower background BEEM current $I_B \approx +40$ fA with a bandwidth of 20 fA at the same $I_T$, no onset in the average of the BEEM spectra (up to 380 spectra taken) has been observed again. Furthermore, the positive background current indicates that holes are collected instead of electrons, which is unexpected for $n$-type Bi$_2$Se$_3$. However, collecting the opposite charge-carrier type can happen due to impact-ionization effects where the hot electron can create an electron–hole pair easily due to the small band gap of Bi$_2$Se$_3$ [82]. This reanalysis of the data after the thesis by Burema, in which the presence of Schottky barrier has been claimed, shows that the expected onsets in $I_B$ can be observed in 10% of the spectra. However, similar onsets in the opposite direction are equally present such that the grand average does not show any clear signatures. Such onsets are thus not related to surpassing of a barrier.

From these measurements, it can be concluded that a Schottky barrier is not likely to be present. From the $I-V$ characteristics, a thermally-assisted-field-emission-like behavior is present where the tunneling contribution gets more apparent upon decreasing the temperature. The origin of a tunnel barrier at the interface is not expected from literature where a transparent junction has been proposed as discussed in section 3.1. A possible explanation for the appearance of such a barrier can be the presence of a contamination layer between the base and collector or the STM contact and the base due to the multiple spincoating and lithography steps. However, it is unclear whether such layers could give rise to tunnel barriers persistent over such large areas that have such a strong temperature dependence. Another reason for observing tunneling can be related to contacting of the STM contact by a spring contact. The spring contact could scratch the topological insulator having a poor adhesion to the substrate, yielding contact with the sapphire or remainders of the Bi$_2$Se$_3$, which is coupled with the collector contact via tunneling. Furthermore, the spring contact is a soft-landing contact, meaning that it makes it connection by the force it exerts on the metal contact where temperature can play an important role. The temperature has, via the thermal expansion coefficient, influence on the position of the spring contact and might yield a tunnel junction with the STM contact pad. Such a junction becomes more transparent towards higher temperatures because then it is in closer vicinity, but not yet completely touching, to the STM contact. This would also give an explanation for the changes in leakage current with temperature.

To check whether the soft-landing contacts could be the reason of the observed tunneling behavior as observed in the two-terminal measurements, an alternative
geometry has been developed, which allows to contact the BEEM and STM contacts through (hard) wire bonding. This requires the separation of the STM contact from the Bi$_2$Se$_3$ collector in order to avoid a short circuit from base to collector. We have tried this by inserting an AlO$_x$ layer and by etching parts of the topological insulator layer away such as to have a remaining insulating sapphire substrate to bond on.

AlO$_x$ insulation layers have been deposited between the thick contact pads and the topological insulator layer. Although it is not fully clear whether this additional layers have been thick enough to avoid the issue of piercing through, we have not been able to reproduce the low leakage current levels, which is necessary in order to measure barrier characteristics with BEEM. From these devices, linear two-terminal $I-V$ characteristics are observed with a leakage current of $\sim 10^{-6}$ A at RT, which lowers maximally to $\sim 10^{-8}$ A at LT. Any BEEM measurements have not been successful because we observe a larger background current up to 40 pA with a large bandwidth that yields large fluctuations in single BEEM spectra. Although we have tried to prevent any issues related to the fabrication and contacting of the device, we have not observed any signatures of a Schottky barrier at the interface via BEEM. This is further confirmed by two-terminal measurements performed on the same devices in another measurement setup, showing linear $I-V$ characteristics up to 77 K. The obvious candidate is that wire bonding still shorts the metal with the topological insulator and therefore the tunneling process as well as the BEEM current collection is distorted by the created parallel channels. In one of the later devices the topological insulator layer underneath the contact pad has been partially etched away such as to avoid such a shortage. However, this solution has not solved the problem of a high leakage current.

### 3.4.2 Solid-state device geometries

Besides the investigation by BEEM, we have performed three-terminal measurements on different topological insulator materials. MBE-grown Bi$_2$Se$_3$ films have been utilized to fabricate nanometer-sized junctions and hot-electron transistors and exfoliated $n$-type and $p$-type BSTS flakes have been used to study the interfaces in topological insulators with reduced doping.

**Nanometer-sized junction area devices** — In the measurements for downsized Pt/Bi$_2$Se$_3$ junctions (figure 3.4), with a low yield of three working junctions, we observe a nonlinear behavior in the three-terminal $I-V$ characteristics with a considerable amount of hysteresis (see figure 3.8a). Furthermore, we observe that the resistance of the junctions decreases with increasing temperature, which indicates that thermally-assisted transport mechanisms play a role at these interfaces. From the low rectification and the nonlinearity, the presence of tunnel barrier seems logical as seen also in the previous section. However, as described earlier, the origin of such a barrier is unclear since charge-depletion layers are not expected that could give rise to tunneling phenomena. In combination with the observed hysteresis that is probably due to charge traps and its unclear temperature dependence, the tunneling signatures could be related to contamination at the interface or to the poor adhesion of the Pt, yielding a small physical separation that can act as tunnel barrier.

Nevertheless, it has been tried to fit these $I-V$ characteristics with the thermally-
Results and Discussion

Figure 3.8: (a) Temperature-dependent three-terminal $I$–$V$ characteristics for a Pt/Bi$_2$Se$_3$ device with junction area of $200 \times 200$ nm$^2$. Positive bias indicates forward bias. (b) Fit of forward bias data at $T = 4.6$ K.

assisted field-emission model under the assumption that a Schottky barrier is present at the interface beyond a bias of 0.2 V; an example of such a fit can be found in figure 3.8b. A brief overview on this model is given by Kamerbeek [96] and more details can be found in the work by Sze [63]. From this model, parameters as the tunneling probability $E_{00}/k_BT$, the degeneracy $\xi$, and the Schottky barrier $\phi_{SB}$ can be extracted for which the values will be discussed as a function of temperature below.

From the fitting, we find that the ratio $E_{00}/k_BT$ decreases from 270–300 at 4.6 K to 5–6 at 300 K, which can be related to a transition in transport mechanism from field emission at low temperature to thermally-assisted field emission at high temperature. Together with the presence of hysteresis, this hints at the presence of a contaminated tunnel barrier rather than a Schottky barrier, which usually shows a clear rectification and is not as symmetric as in the case of tunneling. From the two junctions under consideration, one shows an increase in Schottky barrier $\phi_{SB}$ from 0.5 to 0.7 eV upon increasing temperature whereas the second junction shows a random variation with temperature between 0.5 and 1.0 eV. Such strong changes in the barrier height are not expected since there is no hint of strong changes of the work function of the metal, the electron affinity, or the dielectric constant of the topological insulator with temperature. Furthermore, such high barriers are not at all expected for topological insulator based metal/semiconductor interfaces from the considerations in section 3.1.

The last parameter that can be extracted is $\xi$, which describes the position of the Fermi level $E_F$ with respect to the bottom of the conduction band for degenerate ($\xi < 0$) and nondegenerate ($\xi > 0$) semiconductors and depends on the doping level in the system. It is observed in the measured junctions that $\xi$ becomes less negative by 100 meV with increasing temperature such that $E_F$ moves out of the band gap towards the bottom of the conduction band. Such a large change of $\xi$ is unphysical since this would suggest a thermally (de)activated donor level that would almost double the present charge-carrier density [3]. Furthermore, as described in that work by Brahlek et al., the observation of a nondegenerate semiconductor for the case of the
Studying charge transport at metal/topological insulator interfaces

*n*-type $\text{Bi}_2\text{Se}_3$ where the Fermi level is located inside the band gap is highly unlikely. It is known that Fermi-level pinning to the bottom of the conduction band occurs and an insulator-to-metal transition is therefore difficult to realize. This makes the reliability of the values extracted from this model trickier. Furthermore, the exact origin of the interface barrier is unknown such that the applicability of this model, although describing the data well, can be questioned.

**Three-terminal devices using topological insulator flakes** — We have performed measurements on BSTS-based devices as reported by Hoogeboom [104]. Temperature-dependent Hall measurements confirm the *p*-type and *n*-type character (not shown here). Surprisingly, the measurements show an extraordinarily high mobility on the order of $10^5–10^6 \text{ cm}^2/\text{Vs}$. These surprising results are most probably related to non-ideal shaped BSTS flakes, which leads to improper alignment of the contact leads causing mixing of longitudinal and transversal resistance components. Furthermore, the measurements show a low signal-to-noise ratio, making the extraction of the charge-transport properties and comparison to literature values difficult.

Nevertheless, we have performed three-terminal measurements on these flakes using the geometry as depicted in figure 3.2a. We have realized interfaces between Ti, Ag, and Cu metals with reported work functions ranging from 4.3 to 5.0 eV [62] and BSTS with work function values ranging between 4.95 and 5.20 eV [61]. Within the error of the theoretical values reported, a small Schottky barrier could be present but the presence of an accumulation layer is more likely. This proposition is in agreement

![Figure 3.9](image-url)
Results and Discussion

with the results obtained for \( n \)-type BSTS in which Ohmic behavior was measured for all employed metal contacts. Any temperature dependence in these results can be related to the temperature-dependent resistivity of bulk BSTS. For \( p \)-type BSTS, we found tunneling-like behavior for Ag and Cu contacts (see figure 3.9), whereas for Ti Ohmic behavior consistently over the full temperature range was observed (not plotted here). For the plots shown, it can be seen that the \( I-V \) characteristics change a lot with temperature in a random order. This random order seems to depend on the measurement history that is indicated by the order in the legend. The different measurement cycles for LN\(_2\) cooling and LHe cooling were separated by a month, which could indicate that sample degradation can play a role in the changing properties over time rather than temperature. For the results with the Cu interface, the contact broke down at \( \sim +0.9 \) V at 160 K indicating that the created interface is initially not that stable, which can explain the observed hysteresis too. In comparison to Ti, known for its good adhesion properties, it might be that the adhesion of Ag and Cu on BSTS is not that strong, yielding tunneling contacts locally but this proposition needs additional investigation.

**Hot-electron transistor** — Before the barrier characteristics are considered, the emitter characteristics are discussed which are important for proper hot-hole operation in order to investigate the barrier. Two-terminal measurements have been performed over the tunnel barrier, assuming that this layer is the limiting factor for transport in comparison to the electrodes. From the two-terminal \( I-V \) characteristics, of which an example is shown in figure 3.10a, nonlinear behavior is observed that signifies tunneling behavior of the grown AlO\(_x\) layer. From the temperature dependence, thermally activated behavior is observed, which indicates nonuniformity of the barrier up to some extent. Using Simmons’ model [107], a reasonable agreement is found between data (solid lines) and fit (dashed lines). However, the barrier height \( \phi_B \) and barrier thickness \( t_{TB} \) that are used as fit parameters have an interdependence. The best fit shows barrier heights between 1.5 and 2.2 eV from which a band gap between 3 and 4.4 eV is found, assuming that the band-gap-centered Fermi level of Al\(_2\)O\(_3\) lines up with the Fermi level of the electrodes. This value is a factor of 1.5 to 2 off from single crystalline Al\(_2\)O\(_3\) [108]. Furthermore, a barrier width of \( \sim 1.2 \) nm is found which is 40% lower than intended where the difference can be due to errors in the deposition rate. As shown in figure 3.10b, the area dependence suggests that the actual area is different from that designed, which could originate from misalignment of the respective insulation layer masks that is more crucial for the small area junctions. Such shifts can further lead to the large spread in the fit parameters as extracted from the data in figure 3.10b. Despite the deviations from ideal tunneling behavior, the presence of tunneling from the emitter will lead to a momentum-filtered, hot-hole distribution for investigating the barrier properties.

To investigate the barrier between base and collector, an emitter voltage \( V_E \) is applied and the collector current density \( J_C \) is measured according to the polarities as shown in the inset of figure 3.10c. This means that for positive (negative) \( V_E \) electrons (holes) are injected into the base. The result is found in figure 3.10c where the positive \( J_C \) indicates that indeed holes are collected. Furthermore, a leakage current on the order of \( 10^{-2} \) A is observed within a range of \( V_E = \pm 0.5 \) V, masking the
Figure 3.10: (a) Temperature dependence of emitter current density $J_E$ vs applied emitter voltage $V_E$. The data (solid lines) for a junction with diameter $d = 5 \mu m$ are fitted with Simmons’ model (dashed lines) with a fixed, best value of the tunnel barrier thickness $t_{TB} = 1.2$ nm. (b) Area dependence of emitter current density $J_E$ vs applied emitter voltage $V_E$ at $T = 75$ K. In this fitting, both parameters $\phi_B$ and $t_{TB}$ were floating. (c) Collector current density $J_C$ vs applied emitter voltage $V_E$ at $T = 75$ K for a junction with $d = 150 \mu m$, based on measurement geometry as shown in the inset. (d) Gain $\alpha$ versus emitter voltage $V_E$ obtained from (c). Insets: fits for forward and reverse bias (as defined for holes) according to the Bell–Kaiser theory.

hot-hole characteristics at lower emitter voltages. Due to the presence of an insulating In$_2$Se$_3$:Bi$_2$Se$_3$ (50:50) capping layer, we would not expect a direct transparent interface between base and collector and thus a high leakage current, which suggests that parallel conduction paths are present. Such additional channels can be due to fabrication issues as described in section 3.3.2. However, the exact origin of such a path is unknown and requires further investigation.

Correcting for the emitter’s $I–V$ characteristics gives a better insight into the actual hot-hole characteristics, see figure 3.10d. Plotting the gain $\alpha$ versus emitter voltage $V_E$ reveals that the number of collected holes is relatively small compared to that injected, yielding $\alpha \sim 10^{-4}$. Furthermore, an increase in $\alpha$ is observed for low emitter voltages, which is due to the differences in leakage current levels at both
Conclusions

emitter/base and base/collector interfaces. Nevertheless, a clear onset is observed both at \(-V_E\) (forward hole bias) and at reverse bias. According to the Bell–Kaiser theory (equation 3.1), the barrier height \(\phi_B\) in the forward bias regime can be found by taking \(|\alpha|^{1/2}\) and then finding the onset on the horizontal axis. For the reverse bias, where electrons are injected via the emitter that can excite holes passing the barrier in an Auger-like process, a similar analysis can be performed but now the onset is found by taking \(|\alpha|^{1/4}\) (a more detailed explanation can be found in [83,98]). Such analyses to find the onset can be found in the insets of figure 3.10d. The barrier heights extracted are \(\phi_{B,\text{forward}} = (0.7 \pm 0.2) \text{ eV}\) and \(\phi_{B,\text{reverse}} = (-0.2 \pm 0.2) \text{ eV}\). However, it has to be noted that the exact onsets are difficult to determine since the data is masked by the large leakage current at the base/collector interface, especially on the reverse bias side. The unclear onset due to the large leakage currents close to zero bias has also been observed in other junctions of the device.

The symmetric curve as shown in figure 3.10d could further indicate the presence of a tunnel barrier that is present due to the In\(_2\)Se\(_3\):Bi\(_2\)Se\(_3\) (50:50) capping layer. Here, pure In\(_2\)Se\(_3\) is reported to have a band gap of \(\sim 1.3 \text{ eV}\) [108] and the actual gap will be lower than this value due to the presence of Bi. Instead of a rectifying Schottky barrier, the forward (hole) bias and the reverse (electron) bias would probe the tunnel barrier similarly, which would require an analysis using \(|\alpha|^{1/2}\) for both bias regimes, provided that hot electrons somehow can excite holes in the collector that are registered via \(I_C\). Looking at the left-hand-side inset of figure 3.10d, the onset for the reverse bias would be very similar, yielding a barrier of around 0.7 eV which would be in reasonable agreement with the total band gap of pure In\(_2\)Se\(_3\), indicating that Bi is not of a considerable influence. Additional experiments are needed to clarify this idea as put forward by Burema [105].

3.5 Conclusions

In order to investigate the interface between topological insulators, we have employed BEEM and three-terminal measurements where it initially was assumed that a Schottky barrier would be present. However, as it has become clear from literature, the electron affinity of Bi-based topological insulators is higher than initially assumed, which will lead to an accumulation layer at the topological insulator’s surface, resulting in transparent interfaces. Furthermore, it is reported that electronic states of the metal and topological insulator can hybridize, which can lead to new electrical effects at the interface. In our studies, we have not found any clear (rectifying) signature of any Schottky barrier being present at such interfaces. However, in several cases a tunneling-like behavior has been observed for which its origin is yet unclear. We believe that such phenomena can partially be ascribed the large number of fabrication steps, which can contaminate or structurally change the surface of the topological insulator prior to metal contact deposition. As seen in one of the solid-state devices, the adhesion of some metals on topological insulators is poor, which will influence studies on such junctions and requires a more detailed investigation to rule out such effects. Another tunneling-like effect has been observed in a novel hot-electron transistor architecture, where the capping layer could play an important role. The developed
Studying charge transport at metal/topological insulator interfaces

hot-electron devices based on topological insulators could be an interesting direction to investigate interfaces in more detail. Nevertheless, the absence of a Schottky barrier in these measurements, taking into account the discussed fabrication issues, seems to be in agreement with proposals in literature. This is a positive finding towards the realization of topological-insulator-based solid-state devices with possibilities for low-dissipation transport between a metal contact and the material.

3.6 References


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Studying charge transport at metal/topological insulator interfaces


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