Characterization and partial synthesis of the behavior of resistive circuits at their terminals

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ABSTRACT

The external behavior of linear resistive circuits with terminals is characterized as a linear input–output map given by a weighted Laplacian matrix. Conditions are derived for shaping the external behavior of the circuit by interconnection with an additional resistive circuit.

1. Introduction

In this paper, we consider the characterization and partial synthesis of the behavior of linear resistive circuits at given terminals. The paper is heavily inspired by recent work of Willems and Verriest [1]. In fact, many of the results obtained in Section 3 on external characterization of linear resistive circuits have an analogue in [1]. On the other hand, our approach is somewhat different, certainly in the emphasis on the graph-theoretic content of the results obtained. In particular, we make heavy use of the concept of the (weighted) Laplacian matrix of a graph. It turns out that there are quite a few classical concepts and results available in this area, dating back for example to the original work of Kirchhoff [2], Maxwell and Rayleigh, which are of direct relevance to the questions under study. In particular, we have relied on the excellent book [3], which collects, among many other things, a number of useful classical results on graphs and resistive circuits.

Section 4 is devoted to the partial synthesis of a resistive circuit. Here we consider the problem of shaping the potential/current behavior at the terminals of a given resistive circuit, by interconnecting the resistive circuit through another set of terminals with a judiciously chosen ‘controller’ resistive circuit. We characterize all thus achievable potential/current behaviors. Not surprisingly, this problem is similar to the ‘control by interconnection’ problem as originally formulated in [4], and very close to the problem of ‘achievable Dirac structures’ addressed in [5]; see also [6]. Indeed, the necessary and sufficient conditions for achieving a certain behavior as obtained in [7], see also [8], simplify to necessary conditions in this case. Another necessary condition, which completes the set of necessary conditions to necessary and sufficient conditions, follows from the positivity requirement on resistances.

In applications, resistive circuits with terminals usually appear as subnetworks of circuits containing other elements (capacitors, inductors, diodes). Indeed, one may always identify the resistive subnetwork of any circuit, interconnected to other elements through terminals. The recent paper [9] describes how large resistive circuits occur in the design of very-large-scale integration chips, and how this leads to issues of efficient computation and of the replacement of a large resistive circuit by an equivalent circuit with the same terminals.

2. Preliminaries about circuit graphs

Let us recall some standard definitions regarding graphs, as can be found for example in [10,3,11].

A directed graph $\mathcal{G}$ consists of a finite set $\mathcal{V}$ of vertices and a finite set $\mathcal{E}$ of directed edges; together with a mapping from $\mathcal{E}$ to the set of ordered pairs of $\mathcal{V}$, where no self-loops are allowed. Thus to

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any branch $e \in \mathcal{E}$ there corresponds an ordered pair $(v, w) \in \mathcal{V}^2$, with $v \neq w$, representing the tail vertex $v$ and the head vertex $w$ of this edge. A directed graph is completely specified by its incidence matrix $B$, which is an $(i, e)$ matrix, $i$ being the number of vertices and $e$ being the number of edges, with $(i, j)$-th element $b_{ij}$ equal to 1 if the vertex $i$ is the head of edge $j$, equal to $-1$ if vertex $i$ is the tail of edge $j$, and 0 otherwise. In what follows, ‘graph’ will mean ‘directed graph’ unless stated explicitly otherwise.

Given a graph, we define its vertex space $A_0$ as the real vector space of all functions from $\mathcal{V}$ to $\mathbb{R}$, Clearly, $A_0$ can be identified with $\mathbb{R}^\mathcal{V}$. Furthermore, we define its edge space $A_1$ as the vector space of all functions from $\mathcal{E}$ to $\mathbb{R}$. Again, $A_1$ can be identified with $\mathbb{R}^\mathcal{E}$.

In the context of an electrical circuit graph, the vector space $A_1$ will be the space of currents through the edges in the circuit (with sign following the direction of the edges). The dual space of $A_1$ will be denoted by $A^1$, and it defines the vector space of voltages across the edges. Furthermore, the duality product $\langle B \psi, I \rangle = V^T I$ of a vector of currents $I \in A_1$ with a vector of voltages $\psi \in A^1$ is the total power over the circuit. Similarly, the dual space of $A_0$ is denoted by $A^0$, and it defines the vector space of potentials at the vertices.

The incidence matrix $B$ can be regarded as the matrix representation of a linear map (denoted by the same symbol) $B : A_1 \to A_0$, called the incidence operator. Its adjoint map is denoted as $B^T : A^0 \to A^1$, and is called the coincidence operator.

Although in Kirchhoff’s original treatment of circuit graphs [2], external currents entering certain vertices of the graph were an indispensable notion, this is not always very well articulated in subsequent formalizations of circuits and graphs. We will emphasize this aspect by formally defining an open graph $\tilde{g}$, as obtained from an ordinary graph with set of vertices $\mathcal{V}$ by identifying a subset $\mathcal{V}_b \subset \mathcal{V}$ of boundary vertices. The boundary vertices are the vertices that are open to interconnection (i.e., with other open graphs). The remaining subset $\mathcal{V}_i := \mathcal{V} - \mathcal{V}_b$ contains the internal vertices of the open graph.

Decomposing the incidence operator $B$ as $[B_1 \ B_2]$ with $B_1$ the part of the incidence operator corresponding to the internal vertices, and $B_2$ the part corresponding to the boundary vertices, Kirchhoff’s current laws are now given as

$$ B_1 I = 0, \quad B_2 I = -I_b. \quad (1) $$

Here the vector $I_b$ belongs to the vector space $A_b$ of functions from the boundary vertices $\mathcal{V}_b$ to $\mathbb{R}$ (which is identified with $\mathbb{R}^{\mathcal{V}_b}$, with $\mathcal{V}_b$ the set of boundary vertices). In an electrical circuit graph, the boundary vertices define the terminals of the circuit. In order to have a symmetric notation, we define the vector space $A_b$ as the functions from the internal vertices $\mathcal{V}_i$ to $\mathbb{R}$ (which is identified with $\mathbb{R}^{\mathcal{V}_i}$, with $\mathcal{V}_i$ the number of boundary vertices). Hence $A_0 = A_1 \oplus A_b$ and $A_1 = A_b \oplus A^0$, respectively, so $A^0 = A_1 \oplus A^b$. Kirchhoff’s voltage laws can be written as

$$ V = B^T \psi = B^T_1 \psi_i + B^T_b \psi_b, \quad (2) $$

where $\psi_i \in A^0$ denotes the vector of the potentials at the internal vertices and $\psi_b \in A^b$ the vector of potentials at the boundary vertices.

Kirchhoff’s current and voltage laws result in the following space of allowed currents, voltages, boundary currents and boundary potentials for an open graph $\tilde{g}$:

$$(1) \quad \diamondsuit_{\tilde{g}}(\psi) := \{(I, V, I_b, \psi) \in A_1 \times A^1 \times A_b \times A^b \mid B_1 I = 0, \quad B_2 I = -I_b, \quad \exists \psi_i \in A^0 \text{ s.t. } V = B_1^T \psi_i + B_b^T \psi_b\}. \quad (3)$$

It can be shown [13] that $\diamondsuit_{\tilde{g}}(\psi)$ defines a Dirac structure, called the Kirchhoff–Dirac structure. In particular, $V^T I + \psi_b I_b = 0$ for all $(I, V, I_b, \psi_b) \in \diamondsuit_{\tilde{g}}(\psi)$, expressing that the total power in the circuit is equal to minus the externally supplied power.

**Remark 2.1.** Since $1^T B = 0$, with $1$ being the vector consisting of only ones, it follows [13] that $1^T I_b = 0$, corresponding to the well-known property that the sum of the external currents of a circuit is equal to zero. Furthermore, if $(I, V, I_b, \psi_b) \in \diamondsuit_{\tilde{g}}(\psi)$ then so is $(I, V, I_b, \psi_b + c1)$, for any constant $c$.

### 3. The input–output behavior of resistive circuits with terminals

Consider a resistive circuit with terminals represented by boundary vertices of the circuit graph; see Fig. 1. Without loss of generality, we may assume that the resistances of all the resistors in the circuit are strictly positive. Indeed, whenever there is a resistor with zero resistance, then we remove the edge corresponding to this resistor and equate the vertices at both ends of this resistor. Thus we may as well define the conductances $g_e$ of each resistor as the reciprocal of its resistance $r_e$, that is $g_e := \frac{1}{r_e} > 0$, for every edge $e$ of the circuit graph. Furthermore, in order to streamline the formulation of some results, we will throughout assume that the circuit graphs under consideration contain more than one vertex.

In this section, we want to characterize the relation between the boundary potentials and boundary currents of a resistive circuit; see [1] for closely related results. In the special case where all the vertices of the circuit graph are boundary vertices, this characterization is easy. Indeed, by Kirchhoff’s voltage laws, the vector $V$ of voltages over the resistors is given as $V = B^T_b \psi_b$ (note that $B_b = B$). Furthermore, the vector $I$ of currents through the resistors is given as $I = -GV$, where $G$ is the diagonal matrix with diagonal elements given by the conductances $g_e$, for every edge $e$. Since $B_2 I = -I_b$ it follows that the relation between boundary potentials and boundary currents in this case is given by the linear map

$$ I_b = B_b G B_b^T \psi_b. \quad (4) $$

For any directed graph with incidence matrix $B$, the square matrix $BGB^T$ is known as the weighted Laplacian matrix of the graph (with weights being the diagonal elements of $G$). The weighted Laplacian matrix has many properties, some of which we collect in the following theorem. These properties will be key to the subsequent characterization of the external behavior of any resistive circuit.
Theorem 3.1. Consider a graph $\mathcal{G}$ with incidence matrix $B$. Let $G$ be a positive definite diagonal matrix, of dimension equal to the number of edges. Then

1. The weighted Laplacian matrix $BG^T$ is symmetric, positive semi-definite, and independent of the orientation of the graph. Furthermore, it has all diagonal elements $\geq 0$, all off-diagonal elements $\leq 0$, and has zero row and column sums. Hence the vector $1$ is in the kernel of $BG^T$. If the graph is connected then ker $BG^T = \text{span } 1$; in particular, all diagonal elements of $BG^T$ are $> 0$.

2. Every symmetric positive semi-definite matrix $L$ with diagonal elements $\geq 0$, off-diagonal elements $\leq 0$, and with zero row and column sums can be written as $L = BG^T$, with $B$ the incidence matrix of a graph, and $G$ a positive definite diagonal matrix.

3. If the graph $\mathcal{G}$ is connected, then all diagonal elements of $BG^T$ are $> 0$. Furthermore, all Schur complements of $BG^T$ are well defined, and are symmetric, positive semi-definite, with diagonal elements $> 0$, off-diagonal elements $\leq 0$, and with zero row and column sums. In particular, all Schur complements of $BG^T$ can be written as $BG^T$, with $B$ the incidence matrix of a connected graph $\mathcal{G}$, and $G$ a positive definite diagonal matrix.

Remark 3.2. Parts 1 and 2 are fairly standard (see [3,11] for additional information). $I$ could not find Part 3 in the literature, while its proof is partly based on an argument in [1].

Proof. 1. It is evident that $BG^T$ is symmetric and positive semi-definite. By the property of zero row sums spans $1 \subset \ker BG^T$. Consider the graph without its orientation, and define for this undirected graph the weighted adjacency matrix $A$ as the $\bar{v} \times \bar{v}$ symmetric matrix with $(v, w)$-th element equal to $\bar{g}_{e(v, w)}$ if the undirected edge $e(v, w)$ links the vertices $v$ and $w$, and zero otherwise. Furthermore, define the diagonal $\bar{v} \times \bar{v}$ matrix $D$ with $(\bar{v}, \bar{v})$-th element given as $\sum w: w \sim v \bar{g}_{e(v, w)}$, where $w \sim v$ means that $w$ is linked to $v$ by the undirected edge $e(v, w)$. Then it can be shown ([3], p. 54) that

$$L = D - A. \tag{5}$$

From here, all statements in the first part of the theorem follow, except for ker $BG^T = \text{span } 1$ if $\mathcal{G}$ is connected. This follows from rank $B = \bar{v} - c$, where $c$ denotes the number of connected components of $\mathcal{G}$; see [3,11].

2. Let $L$ be a symmetric positive semi-definite $\bar{v} \times \bar{v}$ matrix with diagonal elements $\geq 0$, and off-diagonal elements $\leq 0$. Then define the undirected graph $\mathcal{G}$ with edge between the vertices $v$ and $w$ if and only if the $(v, w)$-th element of $L$ is non-zero. Furthermore, associate to this edge the weight given by the $(v, w)$-th element of $L$. Then endow the graph with an arbitrary orientation.

3. If the graph is connected, then for each vertex there exists at least one edge linking this vertex to another vertex, implying that each diagonal element of $BG^T$ is $> 0$. We will now show (adopting a proof line in [1]) that the Schur complement of the $(1, 1)$-th element of $BG^T$ is symmetric positive semi-definite, with diagonal elements $> 0$, off-diagonal elements $\leq 0$, and with zero row and column sums. Denote $L := BG^T$. Let $L_{11} > 0$ be the $(1, 1)$-th element of $L$, and let $L^T_{11}$ be the matrix obtained from $L$ by deleting the first row and column. Furthermore, let $I$ be the first column of $L$ minus its first element. Define the Schur complement

$$\tilde{L} := L_{11} - \frac{1}{L_{11}} I I^T. \tag{6}$$

Since all elements of $I$ are $\leq 0$, it follows that the off-diagonal elements of $\tilde{L}$ are also $\leq 0$. It is verified by direct computation that the rows and columns of $\tilde{\mathcal{G}}$ have zero sum, also implying that its diagonal elements are $\geq 0$. Furthermore, $\bar{1} \in \ker \tilde{L}$.

Since the co-rank of a matrix is always greater or equal than the co-rank of any Schur complement of it, and the co-rank of $L$ is one, it follows that the co-rank of $\tilde{L}$ is also equal to one, and that ker $\tilde{L} = \text{span } \bar{1}$. As a consequence, $\tilde{L}$ corresponds to a connected graph, and thus its diagonal elements are again $> 0$. Hence we have proved the claim for the Schur complement of any diagonal element of $L$.

In order to prove the claim for an arbitrary Schur complement, we notice that any Schur complement can be obtained by the successive application of taking Schur complements with respect to diagonal elements. Indeed, consider the Schur complement of $L$ with respect to a leading diagonal block $L_{aa}$ of $L$, say of dimension $\bar{a}$. This can be obtained by first taking the Schur complement with respect to $L_{11}$ to obtain $\tilde{L}$ as above, and then proceeding by taking the Schur complement of $\tilde{L}$ with respect to its first diagonal element, and so on. By repeating this process $\bar{a}$ times we obtain the Schur complement of $L_{aa}$. □

Remark 3.3. It follows from Parts 1 and 2 of the theorem that any symmetric positive semi-definite matrix $L$ with diagonal elements $\geq 0$, off-diagonal elements $\leq 0$, and with zero row and column sums, can be considered as a weighted Laplacian matrix of a certain graph, and conversely. As a consequence, in what follows, any symmetric positive semi-definite matrix with diagonal elements $\geq 0$, off-diagonal elements $\leq 0$, and zero row and column sums, will be succinctly called a weighted Laplacian matrix.

Now let us continue with a general resistive circuit with boundary vertices $V_0$ (corresponding to its terminals), internal vertices $V_i$ and diagonal matrix of conductances $G > 0$. Consider a distribution of potentials over its vertices, such that the corresponding voltages and currents satisfy Kirchhoff’s voltage and current laws. This means that there exist vectors $\psi_i$ (potentials at the internal vertices) and $\psi_b$ (potentials at the boundary vertices) such that the voltages $V$ across and the currents $I$ through the resistors satisfy

$$V = B^T \psi_i + B^T_0 \psi_b \tag{7}$$

$$0 = B I$$

$$-I_b = B_0 \psi_b$$

where $I_b$ are the boundary currents.\[4\] Substitution of the first two equations into the last two yields (see also [9], Eq. (3))

$$0 = B_1 G B_1^T \psi_i + G B_0^T \psi_b \tag{8}$$

Elimination of the internal potentials $\psi_i$ from the first equation and substitution in the second gives

$$I_b = [B_0 G B_1 - B_0 G B_1 B_1^T B_1] \psi_b =: L_b \psi_b. \tag{9}$$

Notice that the matrix $L_b$ in this expression is the Schur complement of the weighted Laplacian of the circuit, given as

$$BG^T = B_0^T \left[ B_1 B_1^T \right]^{-1} G \left[ B_1 B_1^T \right] \tag{10}$$

with respect to the block $B_1 G B_1^T$. This introduces the following theorem.

Theorem 3.4. 1. Consider a linear resistive circuit, having connected circuit graph with internal vertices $V_i$, boundary vertices $V_0$, and diagonal conductance matrix $G > 0$. Then for any boundary potential vector $\psi_b$ there exists a unique internal potential vector $\psi_i$, and unique $I, V, I_b$ such that (7) is satisfied, while $I_b$ is related to $\psi_b$ via (9).
where the Schur complement $L_b$ is well defined, and is a weighted Laplacian matrix.

2. To any weighted Laplacian matrix $L_b$ there corresponds a resistive circuit with diagonal conductance matrix $G > 0$ whose relation between boundary potentials $\psi_b$ and boundary currents $I_b$ is given by the linear map

$$I_b = L_b \psi_b.$$  \hspace{1cm} (11)

In fact, the circuit graph can be taken to be only consisting of boundary vertices. In particular, for any resistive circuit with the relation between boundary potentials $\psi_b$ and boundary currents $I_b$ given by (9) we can construct another resistive circuit consisting only of boundary vertices with the same relation between $\psi_b$ and $I_b$.

**Proof.** 1. It can be shown (see [3], p. 328) that for any $\psi_b$ there exists a unique $\psi_i$ such that

$$B_i(GB_i^T \psi_i + GB_i^T \psi_b) = 0.$$  \hspace{1cm} (12)

Then the boundary current $I_b$ is simply defined as

$$B_b(GB_b^T \psi_i + GB_b^T \psi_b) := I_b.$$ Since the circuit graph is assumed to be connected, by Theorem 3.1 the Schur complement in (9) is well defined, and is a weighted Laplacian matrix.

2. By Theorem 3.1, the matrix $L_b$ in (9) can be written as a weighted Laplacian $B_bG_bL_b^T$, where $B_b$ is the incidence matrix of a graph with only boundary vertices $V_b$ and $G_b$ is a positive definite diagonal matrix. \hfill \Box

**Remark 3.5.** Although any resistive circuit with terminals can thus be replaced by an equivalent circuit without internal vertices, this is computationally not advisable for large-scale resistive circuits. The reason, see [9], is that usually the original network is very sparse, while the Schur complement $L_b$ will be dense. Hence, for a circuit with many terminals this will correspond to a large number of equivalent resistors.

As used in the above proof, for every $\psi_b$ there exists a unique $\psi_i$, such that (12) holds. This unique $\psi_i$ has the following variational characterization; see e.g. [3]. Consider for an arbitrary graph with incidence matrix $B$ and conductance matrix $G$ the following quadratic function corresponding to its weighted Laplacian matrix:

$$R(\psi) := \psi^T B G B^T \psi.$$  \hspace{1cm} (13)

Notice that this function can be rewritten as

$$R(\psi) := \psi^T B G B^T \psi = \frac{1}{2} \sum_{e=(v,w)} G_{e(v,w)} (\psi_v - \psi_w)^2$$

$$= \sum_e e V_e^2,$$  \hspace{1cm} (14)

where $e(v,w)$ is the undirected edge linking vertices $v$ and $w$, and $V_e$ is the voltage across the directed edge $e$ (potential at head vertex minus potential at tail vertex). It follows that $R(\psi)$ equals the total dissipated power in the resistive circuit with conductance matrix $G$. For every fixed $\psi_b$ the function $R(\psi) = R(\psi, \psi_b)$, regarded as a function of $\psi_i$, can be shown to have a unique minimum [3], which is characterized by the zero-derivative condition

$$\frac{\partial R}{\partial \psi_i}(\psi_i, \psi_b) = 2B_i GB_i^T \psi_i = 0.$$  \hspace{1cm} (15)

Since $I = -GV = -GB^T \psi_i$, this condition is however nothing other than Kirchhoff’s current laws $B_i I = 0$ at the internal vertices. Thus we have obtained the following.

**Proposition 3.6.** For every boundary potential $\psi_b$ of the resistive circuit there exists a unique vector of internal potentials $\psi_i$ which minimizes the total dissipated power $R(\psi_i, \psi_b)$.

(3) This is known as Maxwell’s minimum heat theorem, or Thomson’s principle [31].) Furthermore, the quadratic function corresponding to the Schur complement of $B_bG_b^T$ with respect to the block $B_bG_b$, is given by the function

$$R(\psi_b) := R(\psi(\psi_b), \psi_b).$$  \hspace{1cm} (16)

where $\psi_b$ is expressed as a function of $\psi_i$ using (15). It follows that a resistive circuit having the same input–output map $I_b = L_b \psi_b$, but only consisting of boundary vertices (whose existence is guaranteed by Theorem 3.4), has the same total dissipated power as the original circuit. In fact\(^6\)

**Corollary 3.7.** Every resistive circuit with the same input–output map $I_b = L_b \psi_b$ has the same total dissipated power.

3.1. The extension to L and C circuits

The extension of the above results to L and C circuits is straightforward, while the desired extension to RLC circuits is much less clear. (Recall that any RLC circuit can be written as the interconnection of an R circuit, an L circuit and a C circuit, where the interconnection is done via shared boundary vertices; see, for example, [13]).

Completely similar to what we did for R circuits, we can characterize the relation between the boundary potentials and boundary currents of L and C circuits. First consider a C circuit. As in the case of an R circuit, see (8), there exists for every boundary potential $\psi_b$, a unique vector of potentials $\psi_i$ at the internal vertices such that

$$0 = B_c(B_i^T \psi_i + B_b^T \psi_b) - Q_b = B_c(-\psi_i - B_b^T \psi_b),$$  \hspace{1cm} (17)

where $B$ is the incidence matrix of the C circuit, $C$ is a positive–definite diagonal matrix with diagonal elements being the capacitances of the capacitors associated to the edges of the circuit graph, and $Q_b$ is the vector of boundary charges. (Note that by Kirchhoff’s laws the charges corresponding to the internal vertices are all equal to zero.) It follows that $Q_b = L_c \psi_b$, where $L_c$ is a weighted Laplacian matrix (similar to the weighted Laplacian matrix $L_b$ derived for the case of an R circuit; see [9]). By differentiation, we obtain the following relation between boundary potentials and currents:

$$I_b = L_c \psi_b,$$  \hspace{1cm} (18)

with transfer matrix $s L_c$. Note furthermore that the electric coenergy stored at the capacitors can be expressed as the following function of the potentials:

$$H_c(\psi_b) = \frac{1}{2} \psi_b^T B_c B_c^T \psi_b.$$  \hspace{1cm} (19)

In conclusion, the transfer matrix (from boundary potentials to boundary currents) of any C circuit is of the form $s L_c$, with $L_c$ being a weighted Laplacian matrix, and conversely any such transfer matrix can be synthesized by a C circuit; in particular a C circuit without internal vertices. Moreover, the value of the electric coenergy $H_c(\psi_b) = \frac{1}{2} \psi_b^T B_c B_c^T \psi_b$ is the same for any such realization.

In the case of an L circuit with incidence matrix $B$, we obtain that the magnetic energy is given as

$$H_L(\phi) = \frac{1}{2} \phi^T B B^T \phi.$$  \hspace{1cm} (20)

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5 A function $\psi$ satisfying (12) is called a harmonic function on the open graph $G$ with boundary vertices $V_b$. This can be seen to be a direct analogue of the standard notion of a harmonic function with respect to the Laplacian differential operator on a domain with boundary.

6 This is related to what is sometimes [3] called Rayleigh’s principle or the principle of conservation of power.
Theorem 3.1

Consider a connected controller resistive circuit and, with boundary potentials and currents \( \psi_c, i_c \) satisfying
\[
\begin{align*}
\tilde{I}_c &= C \tilde{\psi}_c
\end{align*}
\]
for some weighted Laplacian matrix \( C \).

This controller resistive circuit is interconnected to the plant resistive circuit by identifying the boundary vertices of \( \mathcal{C} \) with the control-boundary vertices of \( \mathcal{P} \) and setting
\[
\begin{align*}
\tilde{\psi}_c &= \psi_c, \quad \tilde{I}_c + i_c = 0.
\end{align*}
\]

This results in the following weighted Laplacian matrix of the resulting interconnected circuit:
\[
\begin{align*}
\left[ 
\begin{array}{cc}
P_{ee} & P_{ec} \\
P_{ce} & P_{cc} + C
\end{array}
\right].
\end{align*}
\]

Hence by Theorem 3.1 the relation between \( \psi_e \) and \( I_e \) of the interconnected circuit is given as
\[
I_e = [P_{ee} - P_{ec}(P_{cc} + C)^{-1}P_{ce}]\psi_e =: (P \circ C)\psi_e,
\]
where the matrix \( P \circ C \) is again a weighted Laplacian matrix.

The problem which we want to address is which weighted Laplacian matrices \( P \circ C \) can be achieved by judicious choice of the weighted Laplacian matrix \( C \). This is answered in the following proposition.

Proposition 4.1. Given a plant resistive circuit \( \mathcal{P} \) as above, with weighted Laplacian matrix \( P \) partitioned as in (22). Let \( S \) be the weighted Laplacian matrix corresponding to a specification resistive circuit with input–output map \( I_e = S \psi_e \). Then there exists a controller resistive circuit \( \mathcal{C} \) such that \( P \circ C = S \) if and only if
\[
S|_{\ker I_{ce}} = P_{ee}|_{\ker I_{ee}} \geq P_{ee} - P_{ec}P_{cc}^{-1}P_{ce}.
\]

Proof. The first condition in (27) follows directly from (25). The inequality constraint on \( S \) comes from the fact that the minimal weighted Laplacian matrix (25) is obtained by taking \( C = 0 \), with corresponding input–output map given by
\[
I_e = [P_{ee} - P_{ec}P_{cc}^{-1}P_{ce}]\psi_e. \quad \square
\]

Let us compare this result with the solution to the ‘control by interconnection’ problem. Specialization of the necessary and sufficient conditions as obtained in [7], see also [8,5], to the case at hand amounts to the following subspace inclusions:

1. \[
\{(I_e, \psi_e) \mid \begin{bmatrix} I_e \\ 0 \end{bmatrix} = \begin{bmatrix} P_{ee} & P_{ce} \\
P_{ce} & P_{cc} \\ P_{ce} & P_{cc} \end{bmatrix} \begin{bmatrix} \psi_e \\ 0 \end{bmatrix} \} \\
\subset \{(I_e, \psi_e) \mid I_e = S \psi_e \}. \quad (28)
\]

2. \[
\{(I_e, \psi_e) \mid I_e = S \psi_e \} \\
\subset \{(I_e, \psi_e) \mid \exists \psi_c, \psi_c \text{ s.t. } \begin{bmatrix} I_c \\ I_e \end{bmatrix} = \begin{bmatrix} P_{ee} & P_{ce} \\
P_{ce} & P_{cc} \\ P_{ce} & P_{cc} \end{bmatrix} \begin{bmatrix} \psi_c \\ \psi_e \end{bmatrix} \}. \quad (29)
\]

These two conditions are readily seen to be equivalent to the two conditions
\[
S|_{\ker I_{ce}} = P_{ee}|_{\ker I_{ee}} \geq P_{ee} \text{ modulo } imP_{ec}.
\]

However, because of the symmetry of weighted Laplacian matrices, these two conditions are actually equivalent. (A similar situation arises in the case of achievable Dirac structures considered in [5].)

A main difference with the situation considered in [7,8] resides in the fact that the ‘canonical controller’ (as introduced in [8]; see also [6]) does not anymore provide a feasible solution, in contrast

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\footnote{Note that a boundary vertex may correspond to different ‘leaves’, i.e., it can be interconnected to a control resistive circuit, while its boundary potential and boundary current are still part of the input–output behavior we wish to shape.}
to the situation considered in [5]. Indeed, by the sign change involved in the physical interconnection of currents, see (24), the canonical controller in this context amounts to the interconnection (via the potentials $\psi_e$ and currents $I_e$) of a copy of the specification resistive circuit with the circuit given by the equations

$$\left[\begin{array}{c}
-I_e \\
-I_c
\end{array}\right] = \left[\begin{array}{cc}
P_{ee} & P_{ec} \\
P_{ce} & P_{cc}
\end{array}\right] \left[\begin{array}{c}
\psi_e \\
\psi_c
\end{array}\right] \quad (31)$$

(note the minus signs!), which corresponds to a sign-reversed copy of the circuit $\mathcal{P}$, where the resistances are replaced by their negative values. Clearly, this does not define an allowed controller resistive circuit $\mathcal{C}$.

5. Conclusions

In this paper, we have applied some classical techniques and results to the problem of the external characterization of resistive circuits with terminals as studied in [1]. Furthermore, we have obtained a basic result on ‘partial synthesis by interconnection’ for such circuits. Although the results are easily extendable to purely inductive or capacitive circuits, the treatment of general RLC circuits remains a topic for further study.

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References