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Electrical characterization of polymer ferroelectric diodes

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July 2010

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Molecular Electronics, Physics of Organic Semiconductors

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Abstract

Photovoltaic measurement is used to directly determine the built-in potential in a phase-separated ferroelectric diode. We observed no changes in built-in potential of the diodes in different polarization states. The remnant polarization of the blend is also measured. We show that the polarization of the blend is preserved upon increasing the content of the semiconductor in the blend composition. The magnitude of the polarization however linearly decreases with increasing semiconductor content. The ferroelectric tunnel junction is the next part of this research. An ultra-thin film of poly(vinylidene fluoride)(P(VDF-TrFE)) was made from solution with spin-coating. Preliminary results show that the presence of pinholes prevents measurement to the tunneling current. Finally, we present studies of non-ferroelectric MIS-diodes with p-type and n-type semiconductors and investigate their ferroelectric polarization behavior.

1. Introduction

In the last two decades, extensive studies have been performed on electronic memories because of the importance of information storage. Memories have many applications like radio frequency identification (RFID) tags. These tags are based on silicon. Recently, organic electronics have attracted great interest because of their lower cost. Using organic materials in RFID can lower the price from 25 cent per conventional silicon-based tag to a few cents organic ferroelectrics. To prevent the loss of information, the embedded memory should be non-volatile. The hysteresis loop of polarization versus external applied field of ferroelectric materials is a potential candidate for non-volatile data storage. The polarization states up and down can be used to store “1” and “0”, respectively. When the external electric field is removed, the polarization state of the memory remains unchanged. As a result, ferroelectric materials are ideal for non-volatile memory applications [1-3].

The ideal memory device has a crossbar pattern wherein a functional material is sandwiched between bottom and top electrodes. In this device, changes of the conductance are probed as the state of the memory. Therefore read-out operation is resistive. A phase-separated blend of organic ferroelectric and semiconductor between two electrodes has recently been reported. This diode showed conductance switching between the two different polarization states of the comprising ferroelectric material [1-3]. The change in conductance was attributed to improvement of charge injection into the semiconductor phase of the blend due to polarization of the ferroelectric phase. Removal of the injection barrier by polarization charges of the ferroelectric is thought to be the origin of bistability.

In this work we first devise an experiment to directly measure injection barrier removal by ferroelectric polarization. Next we show why our measurements were not successful. In the second part of the report, we present our study on the measurement of remnant polarization of the blend diode. Our next attempt is to realize an organic ferroelectric tunnel junction. Challenges in preparing an ultra-thin film of ferroelectric and results from initial electrical measurements are presented. In the last part, we present our study of ferroelectric MIS-diodes. Understanding of the ferroelectric polarization behavior in MIS-diodes is crucial to substantiate the device performance of ferroelectric field-effect transistors. The report ends with an outlook for future studies that are needed in order to understand the behavior of ferroelectrically driven electronic devices.

2. Theory

In this chapter, the concept of ferroelectricity and organic ferroelectrics are first explained. The second part is about conjugated polymers and charge transport through organic semiconductors. Then the theory behind of organic ferroelectric diodes based on phase-separated blends of organic ferroelectrics and semiconductors is considered. In section four, the concept of built-in potential in metal-semiconductor-metal structures is described. The next section is focused on the theory of tunneling in normal and ferroelectric diodes. The final section is about ferroelectric and non ferroelectric MIS-diodes.

2.1. Ferroelectricity and organic ferroelectrics

Ferroelectricity was first observed in Rochelle salt ($\text{KNa}(\text{C}_4\text{H}_4\text{O}_6)\cdot 4\text{H}_2\text{O}$) in 1921[4]. In these materials, electrical properties like dielectric displacement (D) and polarization (P) showed changes with external electric field (E) in the same manner that magnetic field (B) and magnetization (M) vary with magnetizing field (H). Ferroelectric properties were discovered in 1944 in barium titanate and later in ceramics like lead zirconate titanate PZT ($\text{Pb}(\text{Zr},\text{Ti})\text{O}_3$). Eventual widespread applications include in memories, acoustic sensors and transducers [5, 6].

Let us first consider two metal electrodes separated by a very thin layer of vacuum. An applied voltage V on two electrodes with distance d makes an electric field E in vacuum:

$$E = \frac{-V}{d} \quad (2.1.1)$$

This voltage accumulates charges $\pm Q$ on the two metal electrodes. Dielectric displacement (D) is the surface charge density on electrodes:

$$D = \epsilon_0 E \quad (2.1.2)$$

where ϵ_0 is the dielectric permittivity constant in free space. With a layer of insulator between the two metal electrodes, the dielectric constant is increased to ϵ . Then the dielectric displacement will increase for a same electric field due to the polarization induced in the insulator by the metal plates. This induced

polarization attracts more charge in each metal plate of the capacitor. As a result, the dielectric displacement changes to:

$$D = \epsilon_0 E + P \quad (2.1.3)$$

where P is the induced polarization in the insulator. For a normal insulator, this polarization depends only on the external applied field on the capacitor. This polarization changes linearly with electric field.

When a ferroelectric layer is between the two plates of a capacitor, polarization depends only on the history of the applied electric field. Polarization in ferroelectric materials does not change linearly with applied electric field, in contrast to normal insulators. Measurements of dielectric displacement versus applied electric field can be done with a Sawyer-Tower circuit as shown and explained in Figure 2.1.b. Dielectric displacement measurements with different applied electric fields in Figure 2.1.a show clear hysteresis loops. When an electric field is applied to the ferroelectric in a capacitor, polarization is not affected at low electric fields. With increasing electric field, more dipole moments inside the ferroelectric will align with the electric field. Finally, the polarization will be saturated at a field called the coercive field (E_c). In this field, the sign of dielectric displacement will change. After removal of electric field, ferroelectric will keep its polarization, called the remnant polarization. As a result, ferroelectric materials are bistable, meaning they keep their polarization in positive and negative states. Consequently, ferroelectrics are an ideal choice for non-volatile memory applications.

A very well studied organic ferroelectric material is a random copolymer poly (vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) with the molecular structure shown in Figure 2.2. Ferroelectricity exists for 50% -80% P(VDF-TRFE) [8-10]. P(VDF-TrFE) has properties like relatively high remnant polarization, short switching time, thermal stability, radiation tolerance, non-flammability, stiffness and resistance to harsh chemicals [1-3]. The coercive field for thin film P(VDF-TrFE) is 50 MV/m [9, 11].

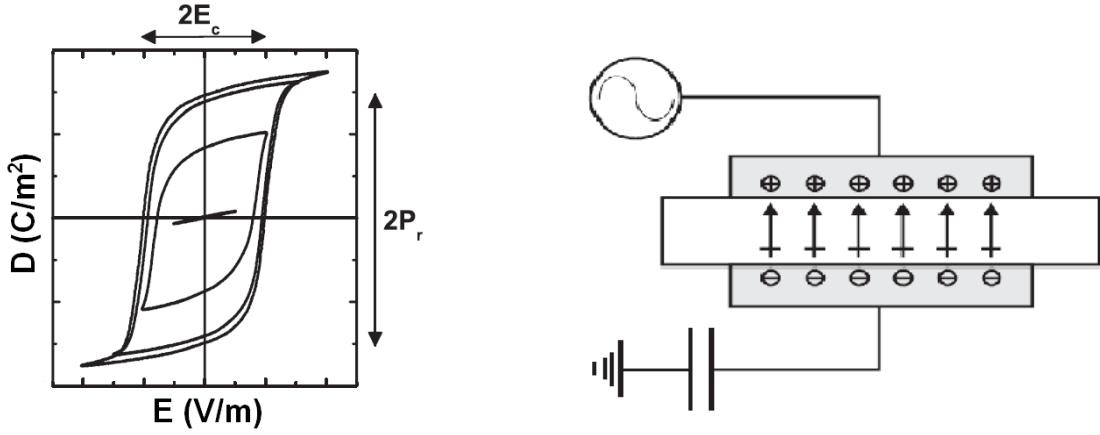


Figure 2.1. (a) Displacement current versus applied electric fields that showing hysteresis loop for a ferroelectric capacitor measured with a Sawyer-Tower circuit. In the bigger loops, the ferroelectric reached saturation polarization at high fields. (b) A sinusoidal voltage signal is applied to a ferroelectric capacitor. The displacement charge is measured via voltage buildup on a reference capacitor that is connected in series. The voltage drop over the reference capacitor is minimized by using a large reference capacitor [7].

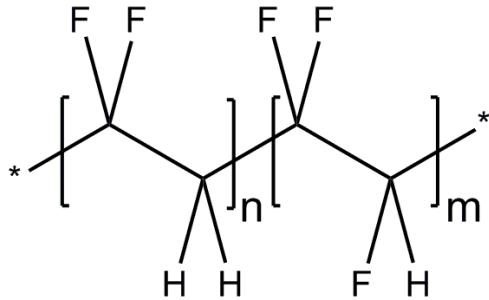


Figure 2.2. Molecular formula of P(VDF-TrFE) [7].

2.2. Conjugated polymers

Most organic semiconductors are conjugated polymers. Conjugation refers to the alternation of single and double bond along polymer backbone. Such a structure enables conductivity along conjugated polymer. The alternation of single and double bond is a result of chemical bonding behavior of the carbon atoms. The carbon atom has four valence electrons. Therefore, it has four half-filled orbital by valence electrons. In conjugated polymers, sp^2 -hybridisation with three orbital will be formed for each carbon atom to make three σ -bonds, two with neighbouring carbon atoms and one with hydrogen. One electron in the P_z orbital remains for each carbon atom. These electrons make a π -bond due to overlap of neighbouring P_z orbitals. These electrons can be delocalized over large distances along the polymer backbone. As σ -bonds are quite rigid and localized, π -bond are responsible for electric conduction in conjugated polymers. The highest occupied molecular orbital in organic materials is called HOMO and the lowest unoccupied molecular orbital is called LUMO. The energy difference between these two levels gives the band gap of materials .With longer polymer chain, the number of π -bond and therefore delocalization length increases. As a result, the band gap of the semiconductor decreases due to greater delocalization lengths, as shown in Figure 2.3. [12].

In inorganic semiconductors, the conduction and valence bands are well defined. Therefore, inorganic semiconductors show band transport model, in which electron transport is in the conduction band and hole transport in the valence band. The charge transport in organic semiconductors is completely different because of disorder. This disorder is due to imperfection of polymer chains. As a result, HOMO and LUMO of polymer have a Gaussian distribution instead of being straight lines. Consequently, charge transport is described as hopping of charge carriers through different conjugated parts of the polymer. The carriers in LUMO and HOMO levels are electrons and holes, respectively. Organic semiconductors with good transport of holes are called p-type. N-type semiconductors are good in electron transport [13].

In conjugated polymers, charge transport via hopping between conjugated parts is phonon-assisted. This is in contrast with the role of phonons in the band transport model in inorganic materials. The theory of charge transport based on hopping from site to site was developed by Miller and Abraham [13].

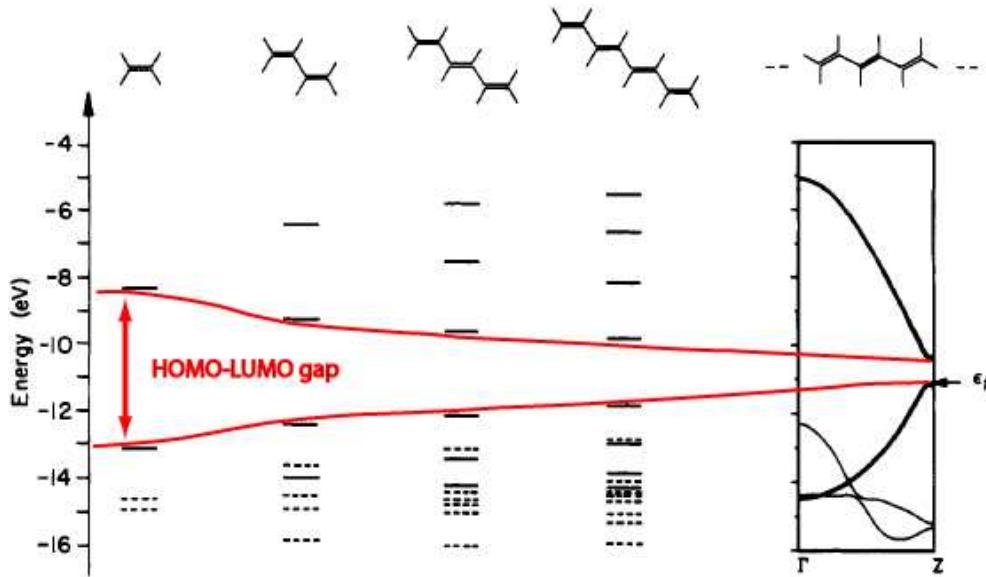


Figure 2.3. An overview of energy levels with increasing chain length, from ethylene to the conjugated polymer polyacetylene [12].

2.3. Interface barriers

In metal-semiconductor contact, an interface barrier exists due to the offset of semiconductor energy levels relative to the Fermi-level of the metal. A metal-semiconductor energy band diagram for large separations is shown in Figure 2.4.a for an intrinsic semiconductor with a defect-free interface. The work function of the metal (Φ_M) is the distance of the metal Fermi level (E_F) from vacuum level (V_L). The HOMO (E_V) and LUMO (E_C) level of the semiconductor are separated by the band gap energy (E_G). The vacuum level and LUMO level of the semiconductor are separated by χ , called the electron affinity. The Fermi level of the semiconductor (E_{FS}) is located in the middle between HOMO and LUMO. The work function of the semiconductor (Φ_S) is the distance of its Fermi level from vacuum level. When metal and semiconductor make contact, their Fermi levels are aligned. This alignment causes band bending in semiconductor.

Figure 2.4.b shows a metal with a higher work function compared to the semiconductor. As a result, hole accumulation at the interface of metal and semiconductor occurs and the energy levels of the semiconductor bend downward. This contact shows an ohmic electron current and an injection limited hole current.

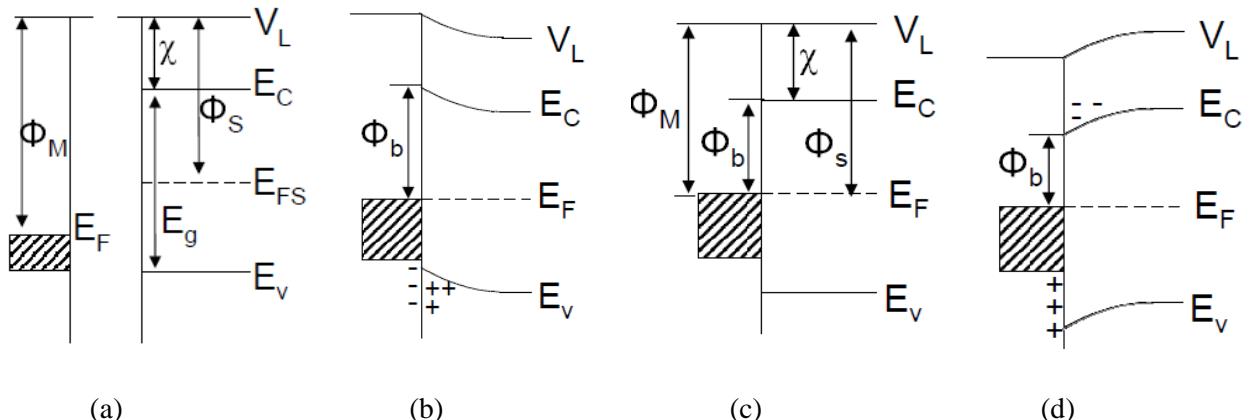


Figure 2.4. Energy diagram for metal- semiconductor contact (a) before contact (b) with a higher metal work function compared to semiconductor with accumulation of holes at the interface, (c) with the same work function for metal and semiconductor, i.e. neutral contact, and (d) with a smaller work function of metal and electron accumulation at the interface [14]

When metal has the same work function as the semiconductor as in Figure 2.4.c, there is not bending of HOMO and LUMO bands after contact. Therefore, contact is neutral.

When the metal has a smaller work function compared to the semiconductor as shown in Figure 2.4.d, electrons are accumulated at the interface of metal and semiconductor in the HOMO level and the energy level of semiconductor bend upward. As a result, metal-semiconductor contact is Ohmic for hole currents and injection-limited for electrons currents.

The current in an organic semiconductor can be dominated either by charge injection or charge transport in the bulk. If the injection barrier is low, the excess charge is maximal and the current depends only on transport in the bulk of the material. The current density J is then determined by the voltage V and the device thickness L , leading to a square dependence on the voltage. This is called space charge limited current (SCLC) and is described by Mott-Gurney's law [15]:

$$J = \frac{9}{8} \epsilon_0 \epsilon \mu \frac{V^2}{L^3} \quad (2.3.1)$$

In this equation, ϵ_0 is the permittivity of vacuum, ϵ the dielectric constant of the polymer and μ the mobility of charge carriers inside the polymer [16].

When there is an injection barrier between the metal Fermi level and the semiconductor energy levels of greater than 0.3 eV ($\Phi_b > 0.3$ eV), contact is injection limited and current through the semiconductor is

called injection limited current (ILC). This current was discussed in Figure 2.2.b for hole injection limited currents and Figure 2.2.d for electron injection limited currents.

2.4. Organic ferroelectric diodes and resistive switches

In this part, a summary of organic ferroelectric diodes with an organic ferroelectric and semiconductor blend is presented.

Figure 2.5.a shows a cartoon of a device in which a phase-separated blend of organic ferroelectric and semiconductor is sandwiched between two electrodes. The blend forms a bicontinuous network of ferroelectric and semiconductor between the two electrodes. The semiconductor polymer most commonly used is poly(3-hexylthiophene)(P3HT), and it is responsible for conductivity in the diode. As mentioned in the last section, choosing metal contacts is important for SCLC or ILC through the semiconductor. In a ferroelectric diode, a metal like silver with work function 4.3 eV is often chosen because it has a high injection barrier of about 0.7eV relative to the HOMO level of P3HT (5.0 eV). Therefore, current through the semiconductor is injection limited [1].

The band diagram in Figure 2.5.b illustrates the unpoled (pristine) state for the ferroelectric. This diagram is for the A-B cross section in Figure 2.5.a.

The ferroelectric polymer is poled with negative bias voltage on the top electrode as shown in Figure 2.5c. As a result, negative charge accumulates at the A-B cross section, holes accumulate in the semiconductor at the interface and the semiconductor HOMO and LUMO bands bend. For thin semiconductor layers, this band bending reduces the injection barrier between the HOMO level of the semiconductor and the Fermi level of the metal. Consequently, the silver metal acts as an ohmic contact for P3HT when the ferroelectric is poled with negative bias voltage.

Figure 2.6 shows current density measurements versus bias voltage. The current density for an unpoled ferroelectric is very low. In negative poling, as shown in Figure 2.5.c, charge injection is improved in the bottom electrode whereas the top electrode remains poor injecting contact. Therefore, in positive bias voltage, there is an increase in current density of at least two orders of magnitude compared to the pristine ferroelectric. For reverse bias, injection should be done from top electrode. Therefore, injection is poor and current density is low in negative bias voltage.

When the ferroelectric is poled positively, the top electrode has improved charge injection whereas the bottom electrode remains a poor contact. As a result, in positive bias, the bottom electrode cannot inject any charge and current density is quite low. In negative bias, the top contact can inject charge and therefore current density increases by about two orders of magnitude.

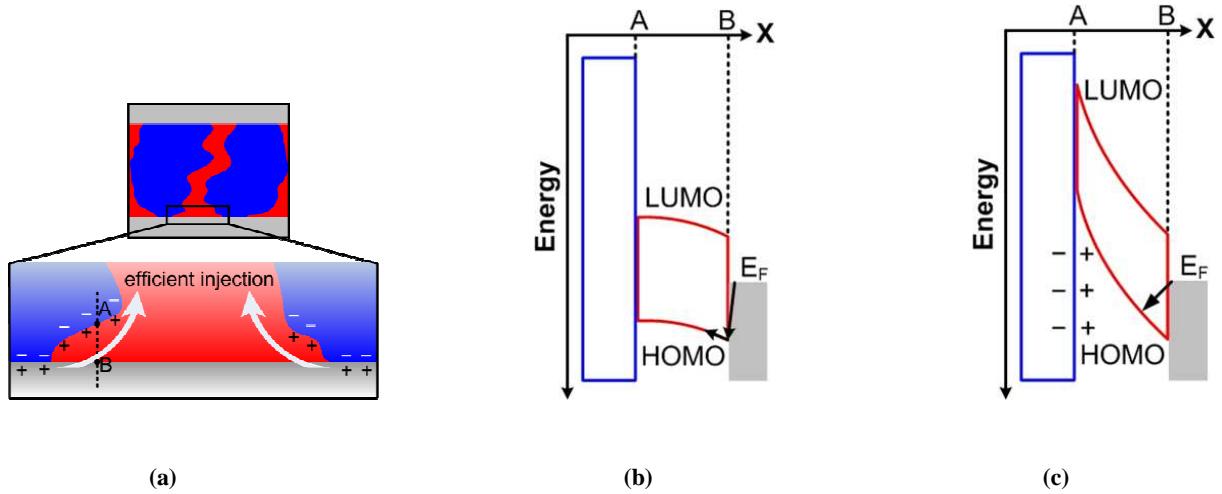


Figure 2.5. (a) Schematic cross section of a diode based on a network of semiconducting and ferroelectric polymers. (b) The band diagram at the bottom silver contact along the cross section A-B for pristine diode (c) and poled diode [1].

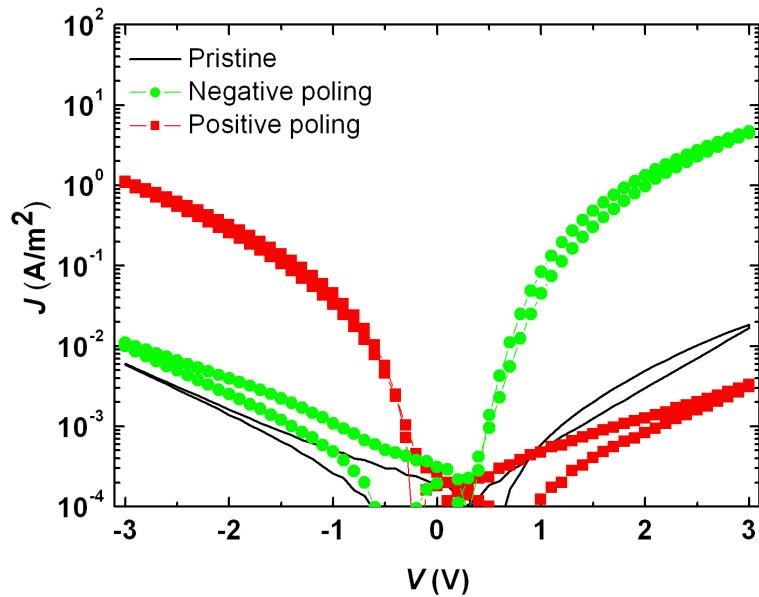


Figure 2.6. J – V characteristics of a diode based on a network of P3HT:P(VDF-TrFE) (1:9) with two Ag contacts, for the pristine film and after positive and negative polarization [1].

2.5. Built-in potential

When a thin layer of semiconductor is sandwiched between two different electrodes, the Fermi level of two electrodes will align with the Fermi level of the semiconductor after contact. This change in Fermi levels causes band bending in the semiconductor. Under illumination of the semiconductor, pairs of electrons and holes will be created. Due to band bending, a voltage called the built-in voltage can dissociate the electron-hole pairs and each charge carrier will be collected in one electrode. This process is a general function of solar cells based on organic semiconductors.

2.6. Tunneling effect

Electron tunneling through a thin layer of insulator is well studied. This effect can be explained by quantum mechanics and is based on the dual wave-particle properties of the electron. When two metals are separated by a very thin layer of insulator or vacuum, tunneling of electrons will occur through the barrier from the Fermi level of one electrode to the other. This effect is a direct consequence of the overlap of the wave functions of electrons in both metals.

In Figure 2.7, a diagram of band model for a metal-insulator-metal interface is shown. A very thin layer of insulator with thickness d is sandwiched between two electrodes, M_1 and M_2 . For a very thin film (a few nm), we expect to see tunneling effects through the insulator according to wave properties of electrons. In this diagram, E_F is the Fermi level, χ is the electron affinity and d is the barrier thickness. Φ_1 , Φ_2 are the barrier height of bottom and top electrodes, respectively. In this diagram, a bias voltage is applied on one electrode while another electrode is grounded. The Fermi level of the electrode under positive or negative bias voltage moves upward and downward, respectively. The difference between the two Fermi levels causes migration of electrons through the narrow barrier from filled states of one electrode to empty states of the other [17-18].

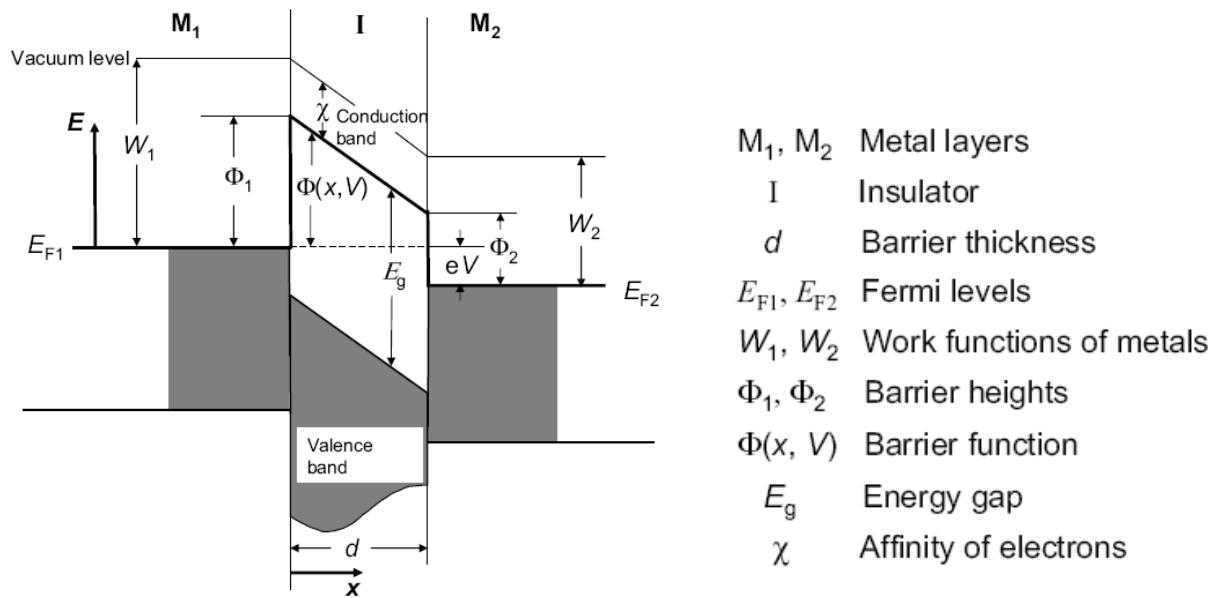


Figure 2.7. Band diagram model for metal- insulator- metal configuration. [19]

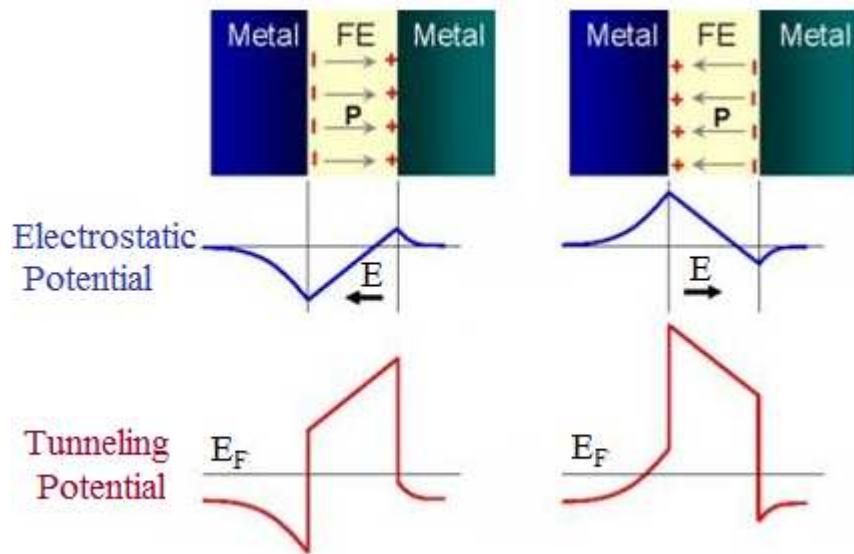


Figure 2.8. Electrostatic and tunneling potential in a FTJ for two opposite polarization orientations [18].

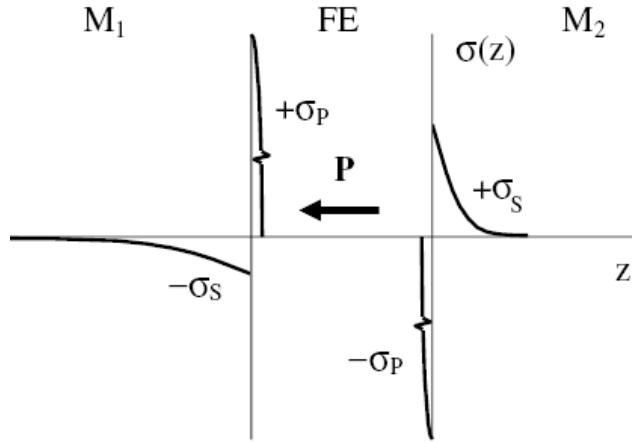


Figure 2.9. Charge distribution in metal-ferroelectric interface at Metal-ferroelectric-Metal structure [18]

2.6.1. Ferroelectric tunnel diode

Now we consider a thin ferroelectric layer in place of a thin insulator. Figure 2.8 shows electrostatic and tunneling potential of two polarization states for an ultra-thin ferroelectric sandwiched between two metals (M_1 and M_2) with different Fermi energy levels. The tunneling potential diagram shows change in tunneling distance for two polarization states. Polarization of the ferroelectric is also taken into account schematically, as illustrated in figure 2.9, where negative polarization charges in the ferroelectric, σ_p , at the interface of ferroelectric and metal (M_1) induce charge distribution, σ_s , at this metal interface. M_1 and M_2 have different screening lengths. The σ_s induced on the metal electrodes at the metal-ferroelectric interfaces therefore leads to creation of two different screening lengths. The screening of the ferroelectric polarization causes variation of the electrostatic potential across the junction in two different polarization states. When different metal electrodes are applied to contact the ferroelectric, the difference in the screening length of the metals, creates an asymmetry in potential profile across the ferroelectric layer upon ferroelectric polarization. As a result, the tunneling current changes through the ferroelectric layer in the two polarization states. The resulting tunneling current is affected by the changes in the screening length in different polarization states. The resistance of the tunnel junction consequently changes by several orders of magnitude, leading to giant electro resistance (GER) [20]. Figure 2.10 shows theoretical current versus bias voltage characteristics of the asymmetric ferroelectric tunnel junction presented in figure 2.8. The mean barrier height of the two electrodes in this plot is changed by about 0.1eV between the two different polarization states [17].

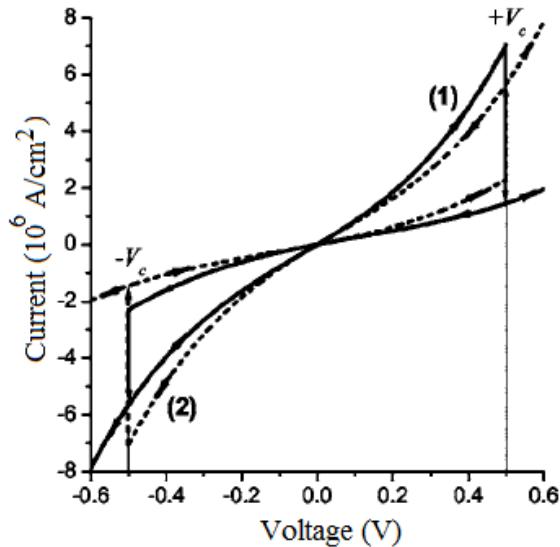


Figure 2.10. Current – voltage curves of an asymmetric ferroelectric tunnel diode in which the source of depolarization is on (1) the biased electrode and (2) the grounded electrode [17]

2.7. MIS-diode

MIS-diode is a metal-insulator-semiconductor structure and it can be considered as a capacitor in which one extra layer of semiconductor is placed between one of the metal plates and the insulator. If a normal insulator is used in this structure, MIS-diode is non-ferroelectric, and when using ferroelectric insulators it is called a ferroelectric MIS-diode. In this section, the capacitance of MIS-diode will be discussed first. Secondly, ferroelectric MIS-diodes are examined.

2.7.1. Capacitance in MIS-diode

The important aspect of MIS-diode studies is capacitance measurements for different bias voltages and frequency. Figure 2.11 shows a schematic of a MIS-diode. When a voltage is applied to the gate electrode, charge carriers will be accumulated or depleted at the semiconductor insulator interface. In Figure 2.12, a p-type semiconductor is sandwiched between an insulator and one electrode plate. When a positive gate voltage is applied, holes accumulate at the interface between insulator and semiconductor. Under negative bias gate voltage, holes at the interface of semiconductor and insulator will be depleted

because of upward band bending. These two regimes are explained in Figure 2.12.b and c and show accumulation and depletion regimes in MIS-diodes. Depletion and accumulation regimes for n-type semiconductor happen for positive and negative gate bias voltage, respectively as shown in Figure 2.13.b and c.

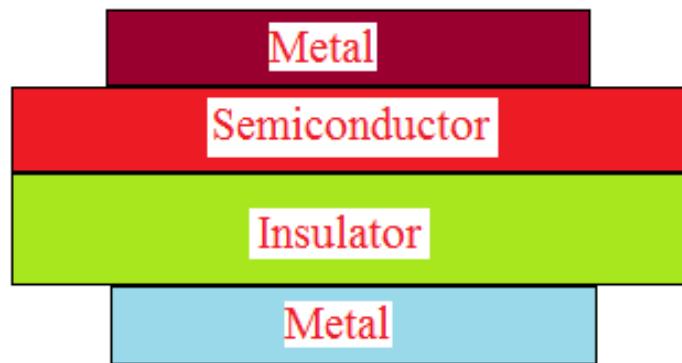


Figure 2.11. MIS-diode schematic

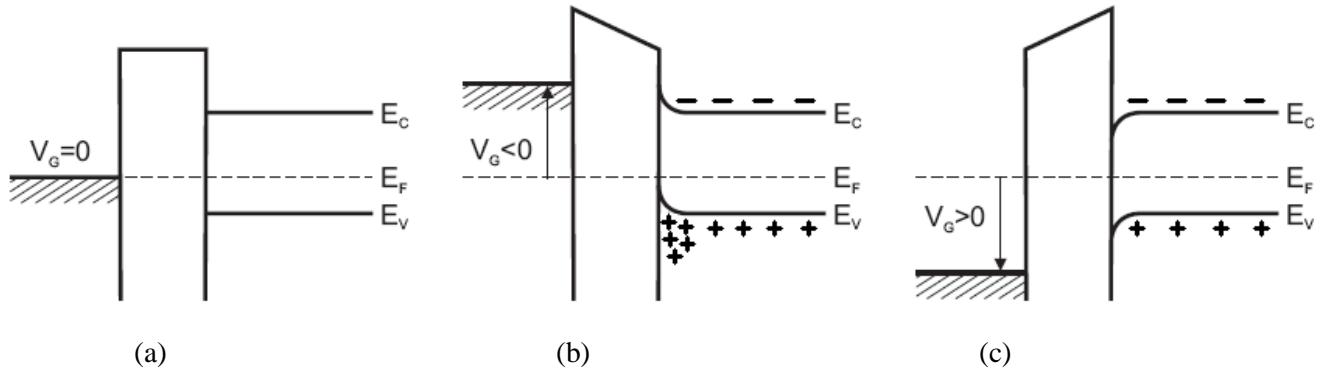


Figure 2.12. Schematic of band energy of MIS-diode at (a) zero gate bias voltage, (b) negative bias voltage, and (c) positive bias voltage for a p-type semiconductor [21]

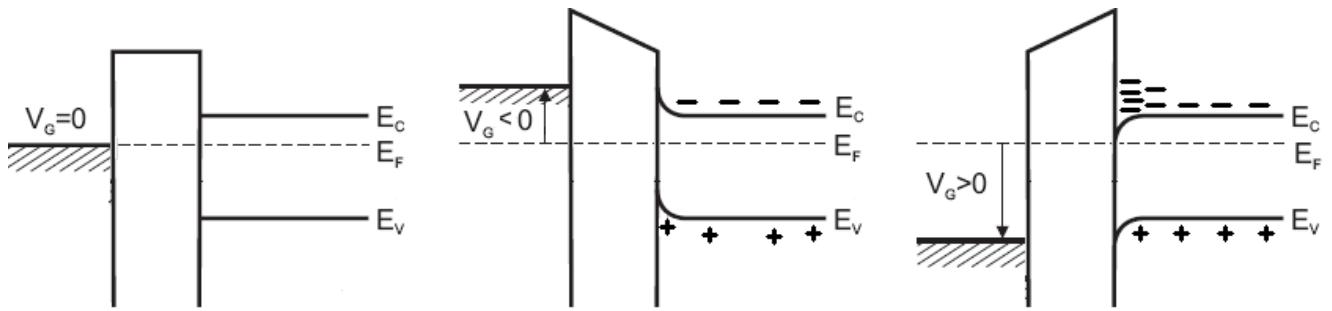


Figure 2.13. Schematic of band energy of MIS-diode at (a) zero gate bias voltage, (b) negative bias voltage, and (c) positive bias voltage for an n-type semiconductor [21]

In the accumulation regime, the p-type (n-type) semiconductor acts like a metal and the total capacitance of MIS-diode is the insulator capacitance. The calculation of capacitance in the accumulation regime of a MIS-diode is as follows:

$$C = \frac{\epsilon_0 \epsilon_{in} A}{d_{in}} \quad (2.7.1)$$

In equation (2.7.1), ϵ_0 is the permittivity of free space, ϵ_{in} the relative permittivity of insulator, d_{in} the insulator thickness and A the device area.

When a MIS-diode is in the depletion regime, holes (electrons) in the p-type (n-type) semiconductor are depleted in the interface of semiconductor and insulator. Therefore, total capacitance can be calculated by considering a semiconductor capacitor in series with an insulator capacitor. As a result, the total capacitance of the MIS-diode is:

$$\frac{1}{C_{tot}} = \frac{1}{C_{in}} + \frac{1}{C_s} \quad (2.7.2)$$

That semiconductor capacitance can be calculated in the same manner as for the insulator. According to equation (2.7.2) and (2.7.1), the total capacitance of MIS-diode in the depletion regime is smaller than that in the accumulation regime.

Figure 2.14 illustrates a measurement of capacitance versus bias voltage for a MIS-diode with a p-type semiconductor. As mentioned above in Figure 2.12, at positive and negative bias voltage, the MIS-diode shows depletion and accumulation regimes, respectively.

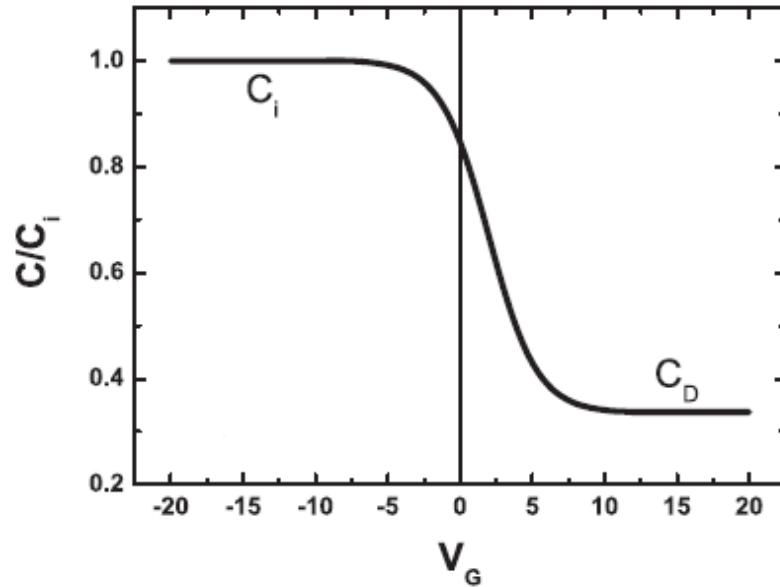


Figure 2.14. A typical C-V measurements for different gate bias voltage in a MIS-diode with a p-type semiconductor

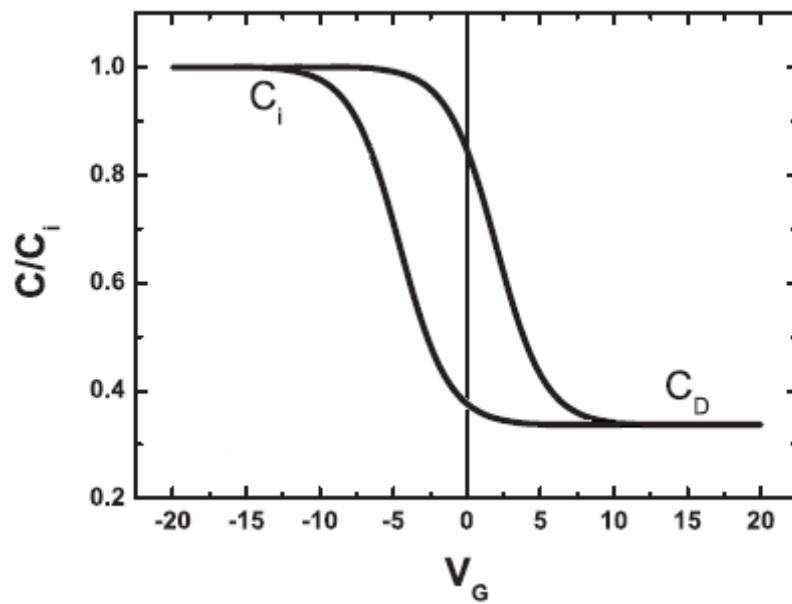


Figure 2.15. A typical C-V measurements versus gate bias voltage in a ferroelectric MIS-diode with a p-type semiconductor

2.7.2. Ferroelectric MIS-diode

A MIS-diode with a normal insulator will return to the flat band condition after removal of the bias voltage. In a ferroelectric MIS-diode, the state of the diode at zero voltage is specified by the polarization of the ferroelectric. As a result, when using a ferroelectric insulator in a MIS-diode, capacitance versus gate bias voltage measurements show hysteresis loops as shown in Figure 2.12. In an ideal ferroelectric MIS-diode with a p-type semiconductor, positive and negative bias voltages result in depletion and accumulation with the hysteresis loop that is located around zero voltage because of the polarization of the ferroelectric.

3. Experiments

3.1. Materials

In this section, the different materials used in this research are introduced first. Then the processing techniques for making devices are explained. Finally, the measurement instruments are mentioned. Figure 3.1 shows the chemical structures of all materials used in this project.

3.1.1. P(VDF-TrFE)

Poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) is a random copolymer of poly(vinylidene fluoride) (PVDF) and poly(trifluoroethylene) (PTrFE). Ferroelectricity can be observed for 50-80 weights percent of VDF monomer. P(VDF-TrFE) has two phases α and β , that later of which is ferroelectric. The coercive field and remnant polarization of P(VDF-TrFE) are 50 MV/m and 60-75 mC/m², respectively. The relative permittivity constant of P(VDF-TrFE) is 11. The P(VDF-TrFE) that has been used in this research, has 65% VDF and 35% TrFE monomers [11, 22].

3.1.2. PTrFE

The chemical structure of PTrFE is similar to P(VDF-TrFE) with the only difference being the exchange of one fluoride atom with hydrogen in P(VDF-TrFE). The physical properties of these two polymers are completely similar to each other. The only difference is that PTrFE is not ferroelectric. These characteristics of PTrFE make it an excellent choice for comparison with ferroelectric P(VDF-TrFE) in different devices such as MIS-diodes and field effect transistors. The solvent that is used for both materials is Methyl ethyl ketone (MEK).

3.1.3. P-type organic semiconductor

The p-type organic semiconductors used in this research are: regio-irregular poly (3-hexylthiophene) (irr-P3HT), regio-regular poly (3-hexylthiophene) (rr-P3HT), Super yellow (SY-PPV).

In regio-regular poly (3-hexylthiophene) (rr-P3HT), all side groups have the same orientation, namely the head- to- tail coupling. P3HT can be dissolved in chloroform. The HOMO level of this polymer is 4.9-5 eV and the LUMO level is 2.7 eV.

In contrast to (rr-P3HT), regio-irregular poly (3-hexylthiophene) (rir-P3HT) has also head- to- head and tail- to- tail coupling that causes interference of the side group with each other and thus more amorphous structure. Super Yellow is a derivative of Poly (*p*-phenylene vinylene) (PPV) with HOMO and LUMO levels of 5.2 eV and 2.8 eV, respectively. It can be dissolved in solvent that can be used with PPV.

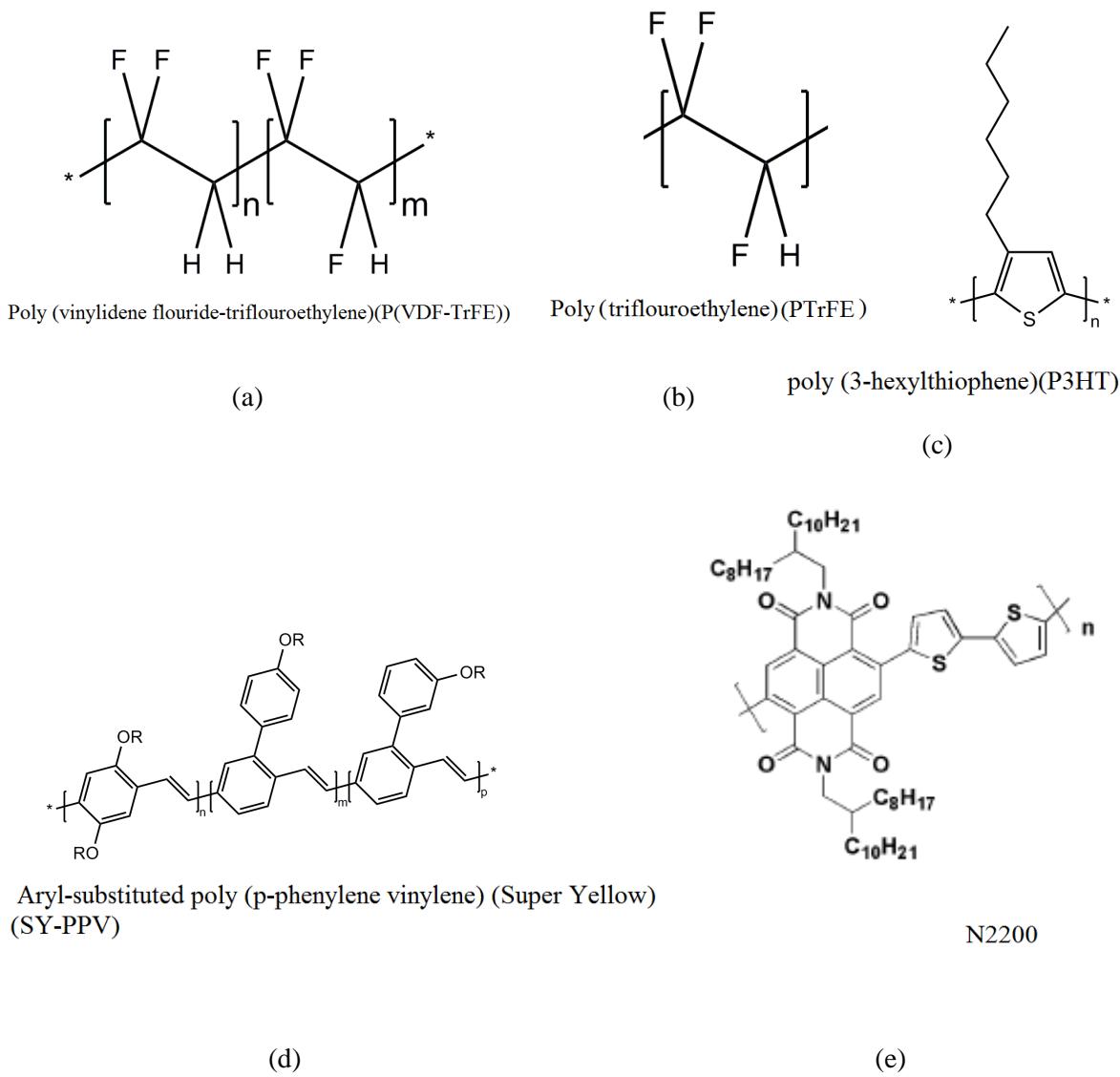


Figure 3.1. Chemical structure of (a) P(VDF-TrFE) (b) PTrFE (c) P3HT (d) (SY-PPV) (e) N2200

3.1.4. N-type organic semiconductor

The n-type polymer that has been used in this project is N2200 from polyera. This polymer has HOMO level of 5.6 eV, a LUMO level of 4.0 eV. The solvent that is used for this material is toluene.

3.2. Device processing

First, the fabrication of ferroelectric diodes based on organic ferroelectric and semiconductor blends is described. Next, the formation of ferroelectric tunnel diode based on an ultra-thin layer of P(VDF-TrFE) sandwiched between two electrodes is discussed. Finally, the fabrication process for non-ferroelectric MIS-diode, using a p-type organic semiconductor (rr-P3HT) and an n-type organic semiconductor is described.

3.2.1. Ferroelectric diodes

A blend of organic ferroelectric P(VDF-TrFE) and organic semiconductor (rir-P3HT or SY) is dissolved with 9:1 weight ratio to a concentration of 20 mg/ml in tetrahydrofuran (THF). Then, 20 nm of silver (Ag) or gold (Au) is evaporated onto a clean glass substrate as a bottom electrode. The solution is filtered with 1 μ m PTFE and is spin-coated onto the metal-coated glass substrate in a nitrogen glove box. After spin-coating, the substrates are annealed in a vacuum oven at 140°C for 2 hours to enhance the crystallinity of P(VDF-TrFE). Finally, top electrode-15 nm barium and then 100 aluminum- is evaporated. A cross-bar pattern is used for the bottom and top electrodes. Device area is 1mm².

The measured film thickness for the blend of P(VDF-TrFE):SY and P(VDF-TrFE):P3HT was 150 nm, with a high roughness comparable with layer thickness.

3.2.2. Ferroelectric tunnel diodes

First, a solution of P(VDF-TrFE) with concentration of 5 mg/ml is prepared in cyclohexanone. The purpose of this low concentration solution is to make an ultra-thin film of less than 10 nm for a ferroelectric tunnel diode. Then, 30 nm of gold is evaporated onto a clean glass or silicon substrate.

After gold evaporation, a filtered solution of P(VDF-TrFE) is spin-coated in air at 60°C solution temperature. Then, the substrate is annealed at 140°C to enhance the crystallinity of the ferroelectric. After the annealing step, a layer of PEDOT:PSS with 90 nm thickness is spin-coated on P(VDF-TrFE). To dry the PEDOT:PSS layer, substrates are put in a vacuum oven at room temperature for 1 hour. Finally, 60 nm of gold is evaporated onto the PEDOT:PSS layer. The device area on glass substrate is 1mm².

For a silicon substrate, first a monolayer of HMDS is formed by dropping several droplets onto the silicon wafer and waiting for a second for evaporation. HMDS makes the surface of the silicon hydrophobic. Hydrophobicity is necessary for depositing the photo-resist onto the silicon wafer after gold evaporation. Photo-resist with thickness of 500 nm is formed by spin-coating on silicon wafer. Then, for 90 second, the substrate with photo resist is put on a hot plate at 95 °C. Afterward, ultra-violet (UV) lithography with special mask is performed. Device areas with different diameters, from 10 µm to 100 µm, are made on the photo-resist. After lithography, we put the substrate in developer for 90 seconds to remove the illuminated part. Then, the substrate is annealed in a vacuum oven at 200°C for 2.5 hours. After annealing, plasma cleaning is performed for 90 seconds with oxygen plasma. Next, the sample is ready for spin-coating of P(VDF-TrFE). The ferroelectric film should be annealed in vacuum oven for 2 hours at 140°C. As a final step, PEDOT:PSS is spin-coated and gold is evaporated as described above.

3.2.3. MIS-diode

Solutions of P(VDF-TrFE) and PTrFE at 30 mg/ml and 50 mg/ml, respectively, are presented in Methyl ethyl ketone (MEK). Silver (Ag) is evaporated to 40 nm thickness on a clean glass substrate. Then, the substrate is put in the oven at 140°C for 10 minutes for better adhesion of silver on the glass substrate. After cooling down, the processing for p-type MIS-diodes and n-type MIS-diodes is as follows:

MIS-diode with p-type semiconductor (rr-P3HT): regio-regular Poly (3-hexylthiophene) in chloroform with 15 mg/ml concentration is spin coated on a silver coated glass substrate in nitrogen glove box to a thickness of about 65-70 nm. Afterward, the substrate is annealed at 140°C for 2 hours in vacuum oven. Then, P(VDF-TrFE) or PTrFE is spin-coated on rr-P3HT in air. The thicknesses for P(VDF-TrFE) and PTrFE are 300 nm and 600 nm, respectively. After annealing again in a vacuum oven at 140°C, silver is evaporated as a top electrode with circular mask with diameter 1-4 mm. The thickness of the top electrode is 800nm.

MIS-diode with n-type semiconductor (N2200): P(VDF-TrFE) and PTrFE solutions with a concentration of 50 mg/ml are prepared in MEK. After filtering with 1 μm PTFE, the solution is spin-coated on to a silver coated substrate in air. Thicknesses of P(VDF-TrFE) and PTrFE layers are 450 nm and 550 nm, respectively. After annealing in a vacuum oven for 2 hours at 140°C, an N2200 solution in toluene (20 mg/ml) is spin-coated on substrates in air. The thickness of N2200 is 140 nm. Finally, a barium electrode with 10 nm thickness is evaporated, and then 400 nm aluminum as a protective layer is coated on barium as top electrode.

In last two sections, MIS-diodes using P(VDF-TrFE) and PTrFE are ferroelectric and non-ferroelectric, respectively.

3.3. Measurements

Photovoltaic measurements of the built-in potential in blends of P(VDF-TrFE):rir-P3HT or SY have been done in a nitrogen glove box with solar simulator in dark state and under illumination. Agilent 8114A pulse generator is used for poling ferroelectric positively and negatively. The blend is illuminated with Steuernagel Solar Constant 1200.

Polarization measurements of blend P(VDF-TrFE): rir-P3HT with different weight ratios of P3HT (1-10%) were performed with a ferroelectric test system (RADIANT). In the software Vision for this system, the PUND (Positive polarization up- negative polarization down) method is used to measure polarization of blend.

Ferroelectric tunnel diode is measured with Keithly 2400 source meter in vacuum in pressure 2×10^{-6} mbar at room temperature. With a Sawyer-Tower circuit, ultra-thin P(VDF-TrFE) was tested for ferroelectric properties. Film morphology images were captured by Atomic Force Microscopy (AFM).

Capacitance versus gate bias voltage was measured with Agilent 4284A Precision LCR Meter. The scan frequency and amplitude are 1 kHz and 100 mV. This measurement was done in vacuum at room temperature. The range of applied bias voltages to the gate was -40 V to +40 V. High potential and high current were applied to the electrode in the insulator part of device and low potential and low current to the electrode in semiconductor part.

4. Results and discussions

4.1. Photovoltaic measurement of built-in potential in blend

The ferroelectric diode based on phase separated blends of an organic ferroelectric (P(VDF-TrFE)) and a semiconductor (rir-P3HT or SY) was described in chapter 2. When a poor injecting contact like silver (Ag) is used as bottom and top contact, current density through the semiconductor is very low in pristine state of ferroelectric, (ILC). When poling the ferroelectric negatively, the current density increases at least two orders of magnitude at positive bias voltage and remains low in negative bias. The reason is improvement of injection for the bottom contact while the top contact is still a poor injector. As a result, the injection barrier between the Fermi level of silver (4.3 eV) and the HOMO level of rir-P3HT (5.2 eV) or SY (5.6 eV) is surmounted up to 1.3 eV in the negatively polarized state of P(VDF-TrFE).

Photovoltaic measurements of built-in potential have been done and results are discussed in this section. The main idea is to find out if the built-in potential of the diodes changes due to changes in the nature of the contacts, and if so, can be directly measured. The device layout is blend of P(VDF-TrFE):rir-P3HT or P(VDF-TrFE):SY sandwiched between Ag or Au as bottom electrode and Barium/Aluminum (Ba/Al) as top electrode.

4.1.1. Built-in potential in P3HT: P(VDF-TrFE) diodes

Figure 4.1 shows the photovoltaic measurement of built-in potential in the blend for positive and negative polarization. Net photocurrent versus bias voltage shows about 0.85eV built in potential for positive and negative polarization. The following conclusions can be drawn from the experimental results:

- 1- rir-P3HT with 10% weight in blend has a very low light absorption
- 2- The current density versus bias voltage shows no change for built-in potential in positive and negative polarization

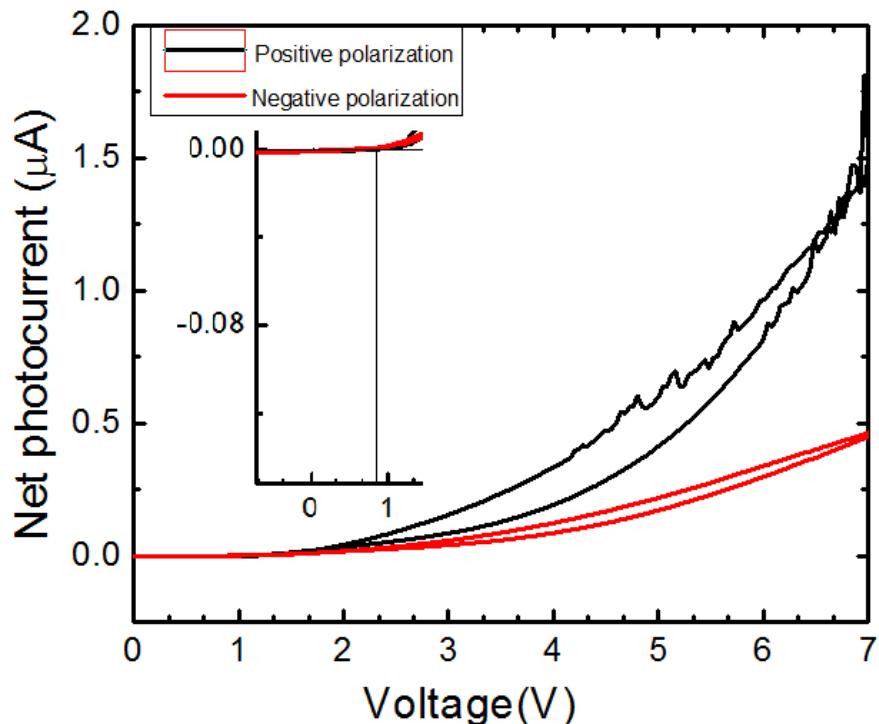


Figure 4.1. Net photocurrent versus bias voltage in positive and negative polarization for device structure Ag(20nm) / P(VDF-TrFE):rir- P3HT / Ba(15nm) / Al(100nm). The inset shows built-in potential from net photocurrent.

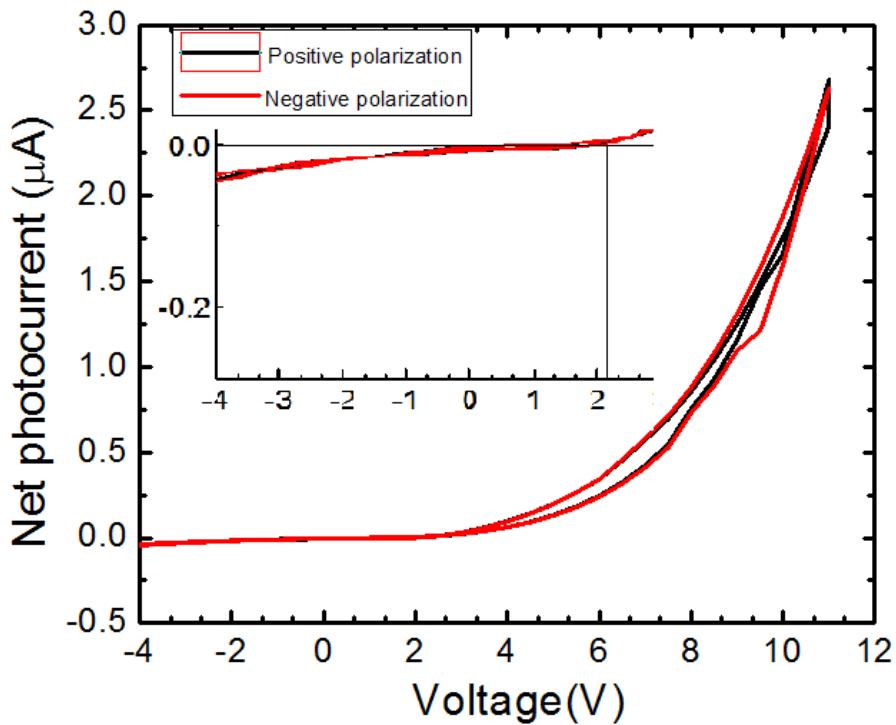


Figure 4.2. Net photocurrent versus bias voltage in positive and negative polarization for device structure Au(20nm) / P(VDF-TrFE):SY / Ba(15nm) / Al(100nm). The inset shows built-in potential from net photocurrent.

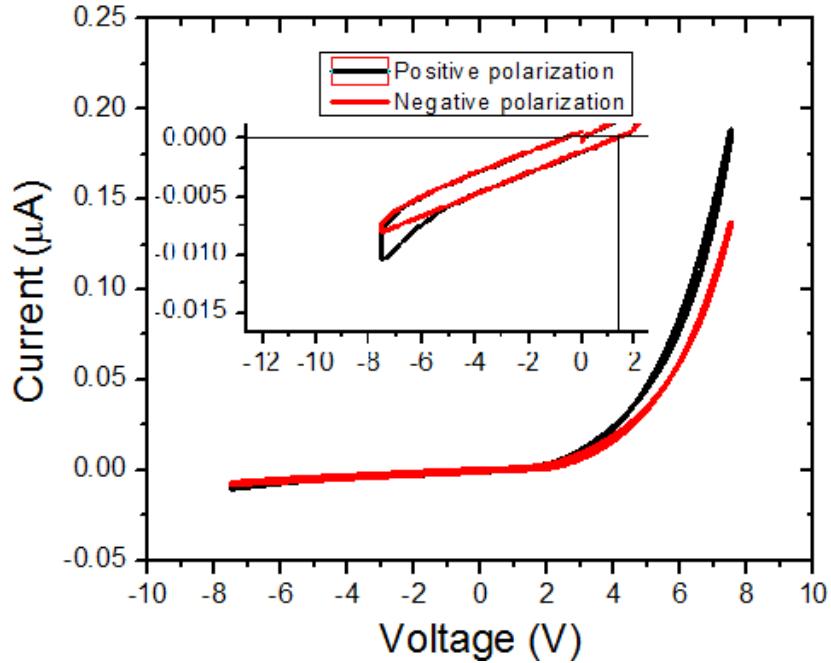


Figure 4.3. Dark current versus bias voltage in positive and negative polarization for device structure Au(20nm) / P(VDF-TrFE):SY / Ba(15nm) / Al(100nm). The inset shows voltage in zero dark current.

4.1.2. Built-in potential in P(VDF-TrFE):SY diodes

In the next step, we replaced the semiconductor component of the blend with a PPV based polymer, SY. The net photocurrent –voltage measurements are shown in Figure 4.2. The reason for using SY is a better absorption compared to rir-P3HT in of the visible range. As a result, no change in built-in potential is observed for positive and negative polarization of the blend. Figure 4.2 shows built-in potential of about 2.15 eV. Observation of the same built-in potential for both polarization directions indicates that polarization of P(VDF-TrFE) does not have any effect on built-in potential. For further comparison, current in dark state versus bias voltage illustrates the same manner as net photocurrent for determining built-in potential as shown in Figure 4.3.

The reason that measurement of the built-in voltage fails in a blend diode is explained in the following. Figure 4.4 shows the current density versus voltage for a blend of P(VDF-TrFE):PFO with Ag or Au as bottom electrodes. The top electrode for both devices is palladium. Devices were measured in the dark. For both devices, the current density in the negative polarization (on-states) starts to flow at voltage that corresponds to the built-in voltage of the device. The slope for current density in on-state crosses voltage axis in 0.1 eV and 0.7 eV for Au / blend / Pd and Ag / blend / Pd, respectively. These values are built in potential and derived by considering the work-function of the electrodes only [2].

It is apparent from Figure 4.4 that the built-in voltage is preserved for the device in the on-state. Hence ferroelectric polarization has no influence. The built-in potential in blend diodes depends on the value of the electrode work-functions. Therefore photovoltaic measurements cannot show the effect of polarization and the removal of the injection barrier.

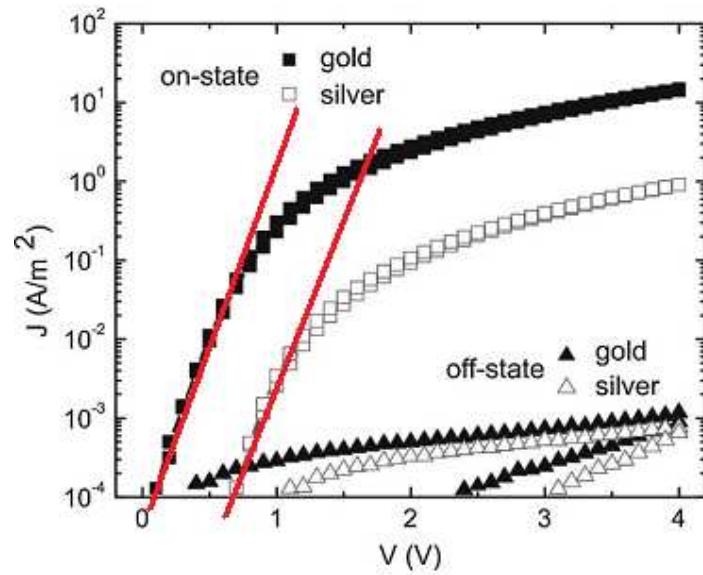


Figure 4.4. Comparison between the on- and off-state current of the blend diodes of 10 wt% PFO and 90 wt% P(VDF-TrFE) fabricated with different anodes; gold (filled black symbols) and silver anodes (hollow red symbols). The slope of these two plots cross voltage axis at built-in potential as shown [2].

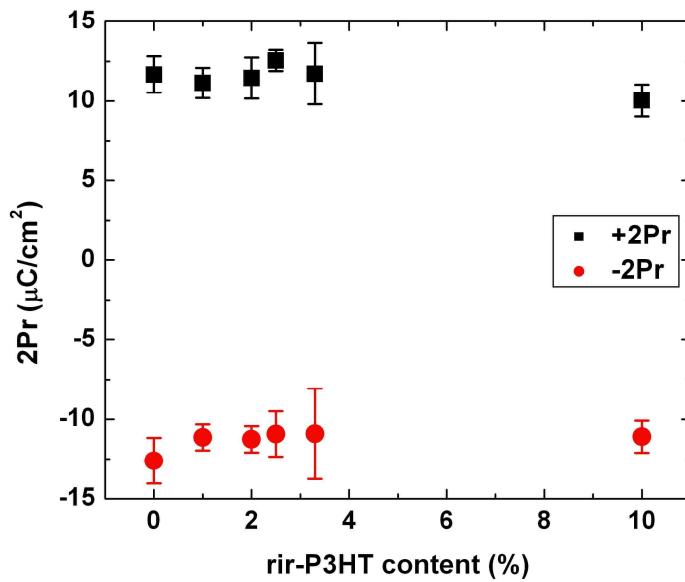


Figure 4.5. Polarization measurement versus rir-P3HT content in blend of P(VDF-TrFE):rir-P3HT

4.2. Polarization measurement in P3HT:P(VDF-TrFE) diode

This part is about polarization measurements for blends of P(VDF-TrFE):rir-P3HT. For a capacitor with a ferroelectric layer between electrodes, the polarization can be measured by the Sawyer-Tower method. In contrast with ferroelectric capacitor, the Sawyer-Tower method does not work out for blend. The reason is the presence of rir-P3HT in the ferroelectric diode, making a leakage current. For this reason, the polarization of blends with different weight percents of rir-P3HT (0-10%) was measured by PUND (Positive Polarization Up, Negative Polarization Down) in a ferroelectric test system. In PUND, three pulses are applied to the blend with an adjustable time interval. The first pulse, polarizes ferroelectric to a known polarization state, then two pulses with opposite polarities are applied to record first remnant+non-remnant and then non-remnant polarization. Figure 4.5 shows polarization measurements on blend diodes of P(VDF-TrFE):rir-P3HT with different weigh percents of rir-P3HT. The results show that, ferroelectricity is preserved in the blend. The negative and positive remnant polarization are about the same and decrease almost linearly with increasing rir-P3HT content of the blend. Consequently, polarization in the blend only depends on the amount of P(VDF-TrFE) in the blend.

4.3. Ferroelectric tunnel junction

The ferroelectric tunnel diode is based on an ultra-thin layer of ferroelectric of a few monolayer thicknesses, sandwiched between two electrodes. In this part of project, an ultra-thin layer of about 7 nm of P(VDF-TrFE) was made by spin coating. The concentration of the solution was 5 mg/ml in cyclohexanone. AFM topography image of the ultra-thin film of P(VDF-TrFE) on a $10 \mu\text{m} \times 10 \mu\text{m}$ scale show pinholes. However, the topography of smaller areas, as shown in Figure 4.6 illustrates a pinhole free ultra-thin film.

Devices with structure Au / P(VDF-TrFE) / PEDOT:PSS / Au were made on silicon substrate by conventional photolithography, with device areas ranging from 0.0001mm^2 to 0.01mm^2 . Most of devices showed electrical shorts because of penetration of PEDOT:PSS particles into P(VDF-TrFE) pinholes. .

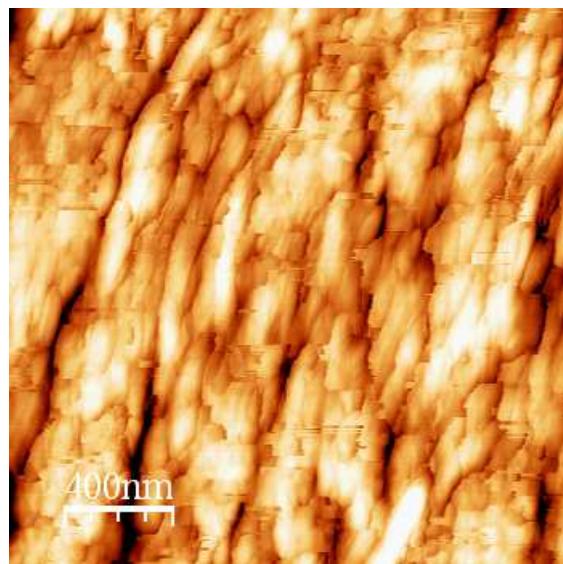


Figure 4.6. Topography AFM image of ultra-thin P(VDF-TrFE) with 7nm thickness. The scanning area is $2\mu\text{m} \times 2\mu\text{m}$, and average film roughness is 5 nm.

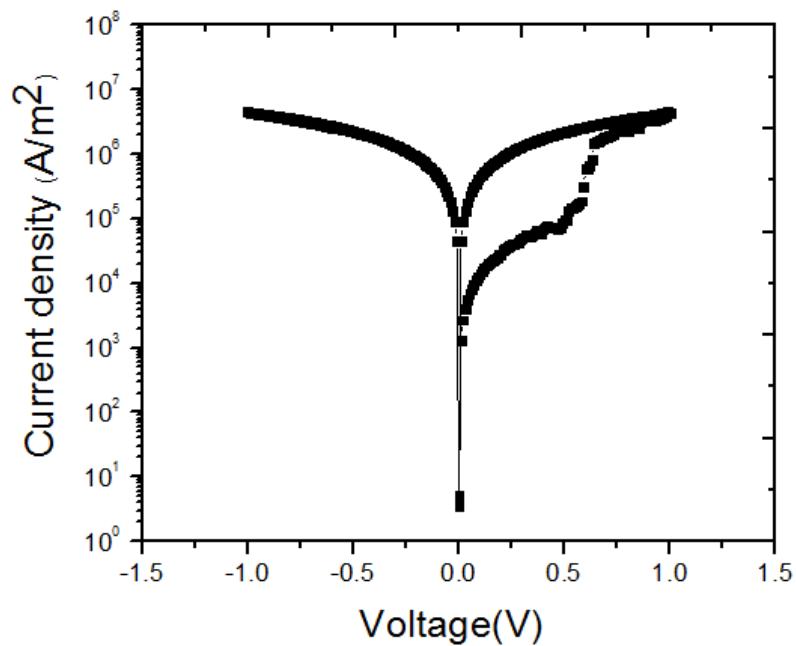


Figure 4.7. Current density versus bias voltage for ultra-thin P(VDF-TrFE) film (7 nm) with structure Au / P(VDF-TrFE) / PEDOT:PSS / Au on photo resist coated silicon substrate

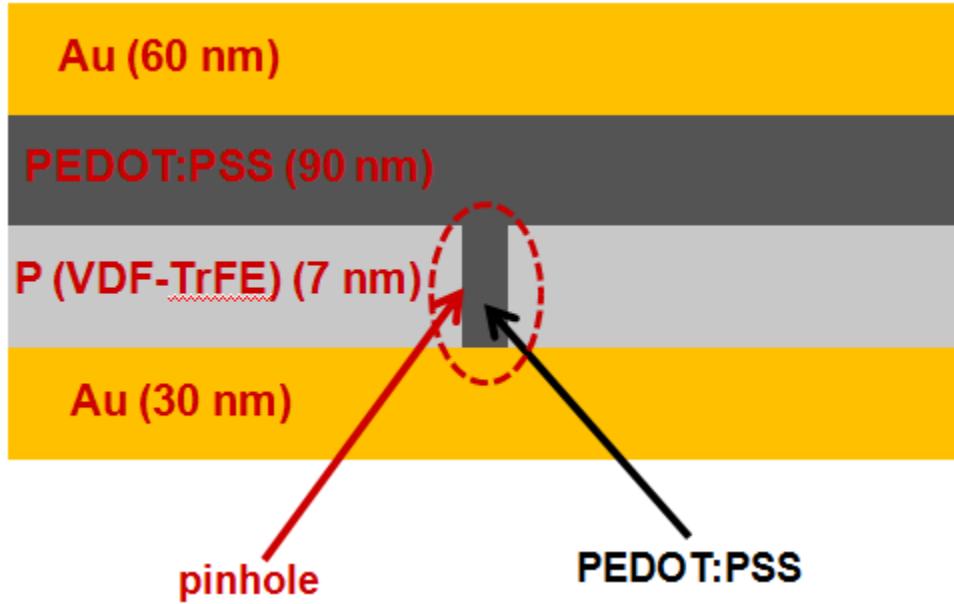


Figure 4.8. Schematic of ferroelectric tunnel diode with structure Au / P(VDF-TrFE) / PEDOT:PSS / Au.

Figure 4.7 illustrates hysteresis in current density versus voltage in positive bias voltage in a device with the smallest area, where the chance of electrical shorts is the least. This figure can prove ferroelectric properties of P(VDF-TrFE) layer and bistability of device resistance. The observed switching voltage of about 0.35 V for 7 nm thickness film is consistent with the coercive field 50 MV/m for bulk P(VDF-TrFE) reported in the literature. Modulation of current can be attributed to the penetration of PEDOT particles into pinholes as shown in Figure 4.8. The final device structure would be similar to that of blend diodes. As a result, negative polarization in P(VDF-TrFE) ultra-thin films at 0.35V modulates the current through PEDOT:PSS in the same manner as in the blend of ferroelectric and semiconductor for ferroelectric diodes. In negative bias voltage, current density does not show hysteresis. The reason is for PEDOT:PSS as top electrode that cannot support compensation charge for P(VDF-TrFE) polarization. Therefore, hysteresis loop is vanished in negative bias voltage because of depolarization in P(VDF-TrFE). Further experiments on this subjects failed due to difficulties in processing of ultra-thin, pinhole-free films of P(VDF-TrFE).

4.4. MIS-diodes based on non-ferroelectric insulator PTrFE

The aim for making non-ferroelectric and ferroelectric Metal-Insulator-Semiconductor (MIS) diodes in this part is to specify ferroelectric field effect transistor (FeFET) performance. Also, the study of the insulator-semiconductor interface in MIS-diodes can give useful outline for using these materials in FeFET. Therefore, the information obtained from MIS-diode can be complementary to information obtained from transistors. A MIS-diode is similar to a capacitor with an extra semiconductor layer between one of the electrode plates and the insulator [23].

In this part, the metal-insulator-semiconductor diode was made with PTrFE as the insulator. A MIS-diode with PTrFE as insulator is a good choice to compare with P(VDF-TrFE)-based MIS-diode performance. PTrFE is a non-ferroelectric polymer with the same physical properties as P(VDF-TrFE). The next two subsections show the results of MIS-diodes using a p-type semiconductor (rr-P3HT) and an n-type semiconductor (N2200).

4.4.1. P-type non-ferroelectric MIS-diode

Figure 4.9 shows capacitance measurement versus bias voltage results for the device structure Ag / rr-P3HT / PTrFE / Ag in a circular device with diameter 4 mm. This plot illustrates the two regimes of accumulation and depletion in negative and positive bias voltage, respectively for the p-type semiconductor. When applying a negative bias voltage on silver on the insulator side, holes will be accumulated at the interface of insulator and p-type semiconductor (rr-P3HT). As a result, the total capacitance of the MIS-diode is the insulator capacitor. The decrease in capacitance at negative bias voltage is because of the permittivity constant dependence of the insulator on the bias electric field. At positive bias voltage, depletion happens at +11V. Calculating the capacitance of PTrFE and rr-P3HT with thickness of 850 nm and 65-70 nm gives 1.44nF and 4.76nF, respectively. The results for capacitance versus bias voltage in Figure 4.9 show good agreement with the calculated ones. Capacitance in the accumulation regime is 1.45 nF and in depletion part is 1.11 nF.

4.4.2. N-type non-ferroelectric MIS-diode

The Non-ferroelectric MIS-diode with n-type semiconductor (N2200) had a different device structure: Ag / PTrFE / N2200 / Ba / Al. Under positive bias, the MIS-diode is in the accumulation regime with only insulator capacitance. The slight decrease in the capacitance in positive bias is again due to the

permittivity dependence on the electric field mentioned in the last section. Under negative bias, the MIS-diode goes to the depletion regime with a decrease in total capacitance. In this regime, MIS-diode behaves like semiconductor and insulator capacitors in series. The depletion occurred at -11 V. Figure 4.10 shows capacitance versus applied bias voltage results for this MIS-diode.

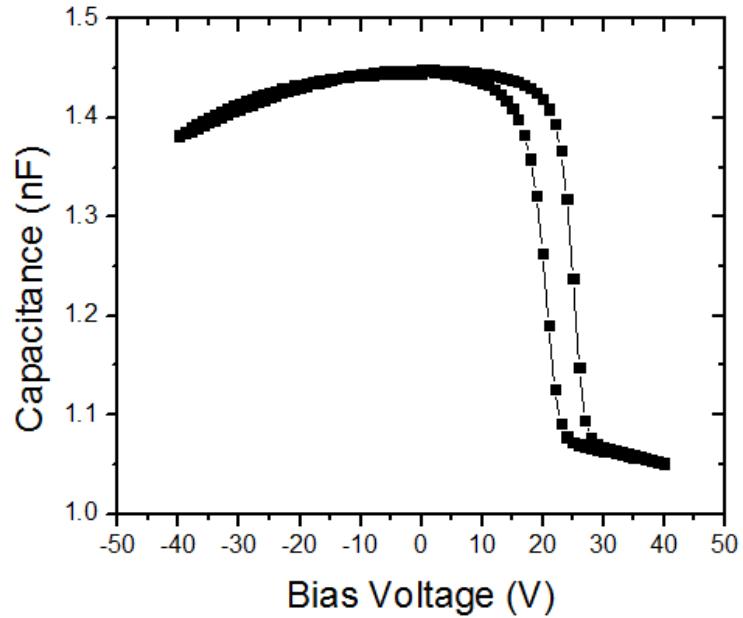


Figure 4.9. Capacitance – voltage measurements for non-ferroelectric MIS-diode with p-type semiconductor (rir-P3HT) in frequency and amplitude scan range 1 kHz and 100 mV (circular device with diameter 4 mm)

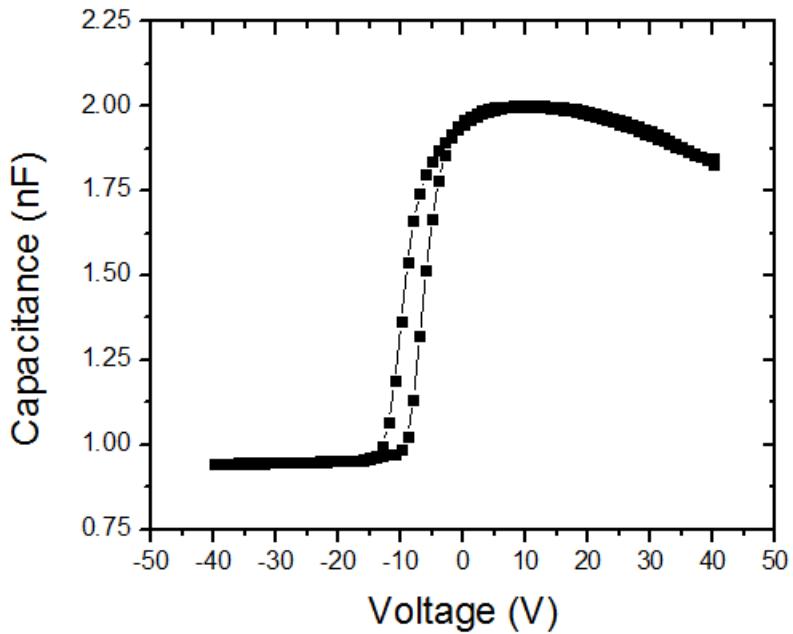


Figure 4.10. Capacitance – voltage measurements for non-ferroelectric MIS-diode with n-type semiconductor (N2200) in frequency and amplitude scan range 1 kHz and 100 mV (circular device with diameter 4 mm)

4.5. MIS-diodes based on ferroelectric insulator P(VDF-TrFE)

After studying of behavior of non-ferroelectric MIS-diode based on the PTrFE insulator with p-type and n-type semiconductors, we turn to the properties of ferroelectric MIS-diode with ferroelectric insulating polymer P(VDF-TrFE). As in the previous section, a p-type semiconductor (rr-P3HT) and an n-type semiconductor (N2200) are used in the ferroelectric MIS-diodes.

4.5.1. P-type ferroelectric MIS-diode

Ferroelectric MIS-diodes with a p-type semiconductor (rr-P3HT) and silver as both bottom and top electrodes show accumulation and depletion in negative and positive bias voltage, respectively. The difference between capacitance behavior at different bias voltages for ferroelectric MIS-diodes versus nonferroelectric diodes is the hysteresis loop. In negative bias voltage, the ferroelectric MIS-diode acts in the same manner as the MIS-diode with PTrFE. This is because of the dependence of permittivity constant of P(VDF-TrFE) to electric field. The ferroelectric gate capacitance with 330 nm thickness is 2.08 nF and for rr-P3HT as mentioned in section 4.4.1. Figure 4.11 illustrates consistency of C-V measurements on the ferroelectric MIS-diode with these values. The device is circular with 3mm diameter.

4.5.2. N-type ferroelectric MIS-diode

For ferroelectric MIS-diode based on an n-type semiconductor (N2200) with device structure Ag / P(VDF-TrFE) / N2200 / Ag, the accumulation and depletion regimes are at positive and negative voltage, respectively. The C-V sweep in n-type ferroelectric MIS-diode seems to be the inverse of p-type. In Figure 4.12, the depletion regime at negative bias voltage shows a hysteresis loop because of the ferroelectricity of P(VDF-TrFE). This behavior can be compared with the non-ferroelectric n-type MIS-diode in Figure 4.10.

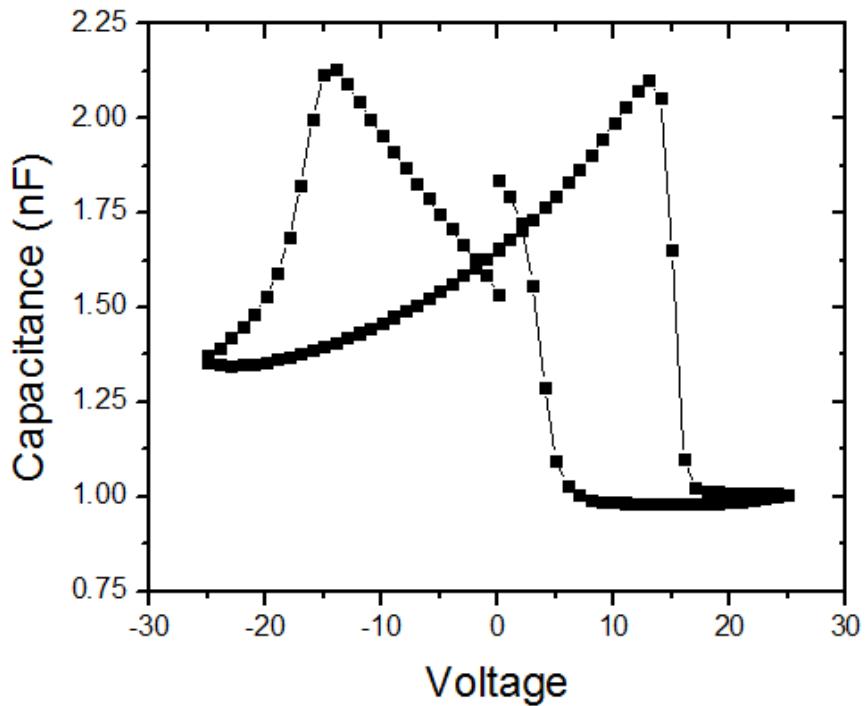


Figure 4.11. Capacitance – voltage measurements for ferroelectric MIS-diode with p-type semiconductor (rir-P3HT) in frequency and amplitude scan range 1 kHz and 100 mV (circular device with diameter 3 mm)

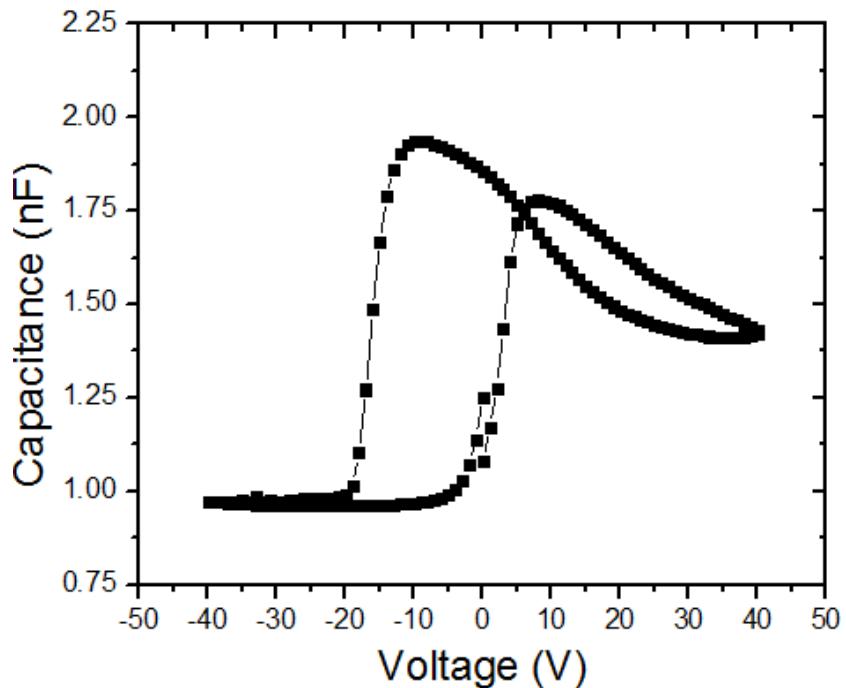


Figure 4.12. Capacitance – voltage measurements for ferroelectric MIS-diode with n-type semiconductor (N2200) in frequency and amplitude scan range 1 kHz and 100 mV (circular device with diameter 4 mm)

5. Conclusion

Photovoltaic measurement of the built-in potential of blends of P(VDF-TrFE):rir-P3HT and P(VDF-TrFE):SY is not the proper method to characterize built-in potential. The reason is that in the blend diodes, the built-in potential is determined only by the work function of the metal electrodes. Ferroelectric polarization, although it modulates the injection barrier for charge injection, has no influence on the device built-in potential.

The polarization of blends of P(VDF-TrFE):rir-P3HT with different weight percents of rir-P3HT (0-10%) was measured with a pulse-based technique, the PUND method. The measurements showed that the ferroelectricity of blends with different weight percents of rir-P3HT is preserved and its magnitude decreases linearly with increasing rir-P3HT content.

In the third part, the ferroelectric tunnel junction was studied. Ultra-thin films of ferroelectric polymer were prepared. AFM showed that a film thickness of 7 nm can be reached. Ultra-thin films suffer from the presence of pinholes. However if devices can be made on very small areas, the chance of having pinholes is minimized. *I-V* sweeps of devices show either electrical shorts or modulation of current injection into PEDOT:PSS. Both of these are attributed to the presence of pinholes.

The last part of this project concentrated on ferroelectric and non-ferroelectric MIS-diodes based on using P(VDF-TrFE) and PTrFE. P-type and n-type semiconductors were used in both types of MIS-diodes. The *C-V* measurement for non-ferroelectric MIS-diodes using a p-type semiconductor has shown accumulation and depletion regimes in negative and positive bias voltage, respectively. Inverse behavior was obtained for the non ferroelectric MIS-diode with n-type semiconductor.

Ferroelectric MIS-diodes with p-type and n-type semiconductor have the same behavior in their *C-V* sweep as non-ferroelectric MIS-diodes, except for the existence of hysteresis loops because of the ferroelectricity of P(VDF-TrFE). In the accumulation regime, the ferroelectric is polarized. Compensation charges are provided by the semiconductor. Using an n-type or p-type semiconductor stabilizes only the positive or negative polarization state of the ferroelectric, respectively. The opposite polarization of the ferroelectric in either case is unstable due to the lack of compensation charges. Thus the ferroelectric depolarizes.

6. Outlook

First, depolarization measurements on blends of P(VDF-TrFE):rir-P3HT with an n-type semiconductor are considered. In this part, an ad layer of n-type will be inserted between the bottom electrode and blend in a ferroelectric diode. The polarization in the blend can be measured for different thicknesses of n-type semiconductor. In this way, one can unambiguously study the depolarization mechanism in blend diodes.

The next subject that can be studied is ferroelectric diodes based on blends of P(VDF-TrFE) and n-type semiconductor.

Also, studies on ferroelectric tunnel diode based on organic material are quite interesting. Recently, many groups in the world have studied on ferroelectric diodes based on organic and inorganic materials. The main issue in this part is to make an ultra-thin film of P(VDF-TrFE) defect-free with a few nanometer thicknesses. There are some solutions for removing pinholes in P(VDF-TrFE) ultra-thin films. One is to use alkanethiols to form self-assembled monolayer. The thiol molecule will attach to the gold surfaces that are exposed in the pinholes. In this way a thin barrier is created between the bottom electrode and the contacting PEDOT:PSS top electrode. Another method can be mixing PS (polystyrene) with high-molecular weight in P(VDF-TrFE) solution.

7. Acknowledgement

First of all, I would like to thank Paul for accepting me into his group. I had an opportunity for doing my research in a friendly environment and the nicest group at this university. Whenever I asked questions about my research, he always had very nice comments. I like to continue my acknowledgement with Dago; we always had very nice work meetings with nice discussions.

The special part of my acknowledgement belongs to my supervisor Kamal, who helped me a lot during my research. I really thank you for your help and always hope the best for you in your entire life. I would also thank Auke and Johan for giving nice comments. I could learn many things from their advice during my research. I thank Jan because of his effort for making very nice environment in clean room for students and PhDs. Finally, I acknowledge the entire group member because of helping me every time I asked them.

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