Spin caloritronics in magnetic/non-magnetic nanostructures and graphene field effect devices
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DOI:
10.1038/nphys2743

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Document Version
Publisher's PDF, also known as Version of record

Publication date:
2015

Link to publication in University of Groningen/UMCG research database

Citation for published version (APA):
Dejene, F. (2015). Spin caloritronics in magnetic/non-magnetic nanostructures and graphene field effect devices [Groningen]: University of Groningen DOI: 10.1038/nphys2743

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Download date: 29-10-2017
Appendix A

Fabrication techniques

The devices studied in this work were fabricated on three types of wafers: [1] heavily doped 2” Si wafers with 300 nm SiO$_2$ layer (for chapters 3, 4 and 5), [2] heavily doped 5” Si wafers with 500 nm SiO$_2$ layers (in chapter 7), and [3] 2” single-crystal Yttrium Iron Garnett (YIG) with a 200 nm thickness that was grown by liquid phase epitaxy on a 500 $\mu$m thick (111) Gd$_3$Ga$_5$O$_{12}$ (GGG) substrate (in Chapter 6).

A.1 Deep-UV Optical lithography

Structures as small as 1$\mu$m can be patterned using the EVG-620 Deep-UV Mask Aligner system. In this step, contact-pads and positional markers for use in the electron beam lithography (EBL) step are patterned following the recipe described below.

1. **Cleaning substrate**: Contamination from the surface of the wafer is cleaned using warm Acetone followed by rinsing in 2-isopropanol (IPA) and di-water. The wafer is then baked on a hot plate at 180 °C for 120 seconds.

2. **Resist spinning**: The photoresist ZEP-520 in anisole is spun at 3000 RPM for 60 seconds to obtain a thickness of $\sim$300 nm and the wafer is baked for 90 seconds on a hot plate at 180 °C.

3. **Deep-UV exposure**: After loading the Cr-coated glass mask into the EVG-620 system and bringing the resist coated wafer in contact with the mask (Cr side facing down), deep-UV exposure of the resist with a dose of 700 mJ cm$^{-2}$ transfers the patterns of the mask to the sample.

4. **Development**: To dissolve the exposed areas of the polymer, the wafer is immersed in n-amyl acetate for 60 seconds and immediately rinsed in IPA for 30 seconds.

5. **Metal deposition**: Using the Temescal FC-2000 e-beam evaporator a 5 nm thick Ti adhesion layer and an 80 nm thick Au layer is deposited at a rate of 1 – 3 Å/sec at a base pressure of $1 \times 10^{-6}$ Torr.
A. Fabrication techniques

(a) (b) (c)

Figure A.1: (a) Optical microscope image of Deep-UV lithography-patterned device (2×2 mm² in dimension) showing four positional markers for e-beam lithography, sixteen contact pads running to a 100μm×100μm device region. (b) A close-up scanning microscope image of a device prepared by e-beam lithography and thin film deposition methods. The four crosses surrounding the device are used to align consecutive EBL steps (12 steps in this case) with an accuracy of < 10 nm. (c) An example of one of the devices (presented in chapter 4).

6. **Lift-off**: The wafer is immersed in a preheated PRS-3000 solvent (at 90 °C) for 10-15 minutes, the resist along with the metal film (in the unexposed regions) is removed. Gentle ultrasonication can be employed if necessary. The wafer is finally cleaned in IPA.

7. **Cutting**: The samples are cut using a precision diamond scriber system (RV-129) into a required dimension (often 3×4 arrays of each 2×2 mm² devices as shown in Fig. A.1)

8. **Plasma etching**: The lithography process sometimes leaves behind some polymer residues on the wafer [see, for example, the polymer bubbles in Fig. A.1(c)]. These residues, which may cause sticking or line breakage problems, can be removed using O₂ plasma cleaning (power: 100 W, flow: 25 sccm) for 1 or 2 minutes.

A.2 E-beam Lithography (EBL)

Unlike optical lithography, EBL provides the capability of fabricating nanostructures with dimensions only limited by the thickness of the resist and the interaction of electrons with the resist. With the Raith e-Line 150 EBL system dimensions as low as
20 nm could be fabricated. The procedures followed in the fabrication of nanodevices studied in this work are described below:

1. **Resist spinning:** An EBL resist (PMMA 950 K with 2-4% solid content dissolved in ethylactate) is spun at 4000 RPM and baked on a hot plate at 180 °C for 90 seconds. Depending on the solid content the thickness of the final resist ranges from 70 nm (2% solid content) to 270 nm (4% solid content). Note that for an insulating substrate such as the YIG/GGG charging due to e-beam exposure must be avoided. Two methods often employed are (i) sputtering a thin layer of Au or (ii) spin coating a very thin conducting polymer layer on the PMMA resist. In this thesis the latter method is used where aqueous based conductive polymer (aquaSAVE-53za) is spun on top of the PMMA at 6000 RPM followed by a short baking on a hot plate at 180 °C for 30 seconds.

2. **E-beam exposure:** An automatic write-field alignment technique using predefined cross-shaped markers (shown in Fig. A.1(b)) is employed to perform the exposure. A beam of electrons, accelerated to an energy of 30kV and through a 10 µm aperture (beam current: 0.035 nA), is scanned over the sample. Typically, an area does of 450 µC/cm² is required to clear the polymer in the development step. One special property of PMMA is that, when exposed to more than 20 times the clearing dose, it cross-links and become difficult to remove with a standard lift-off technique. This special property is used in chapters 3 to 5 for the fabrication of the nanopillar spin valve devices as discussed in the next section.

3. **Development:** Dip in a IPA:MIBK mixture (1:3 by volume ratio) for 30 seconds, rinse in IPA for another 30 seconds and finally spin or blow dry. Note that for the YIG samples, the aquaSAVE layer must be removed using di-water before performing the regular development step described above.

4. **Metal deposition:** Prior to the deposition of any metals using the TFC-2000 e-beam evaporator, surface oxides or polymer residues from previously deposited metals are removed using an Ar⁺ ion-milling (etching) technique. Typical etch rates, for instance, for Permalloy are 5-6 nm/min for the following settings: beam voltage of 500 V, acceleration voltage of 200 V, discharge voltage of 50 V, beam current of 14 mA and Ar pressure of $2 \times 10^{-5}$ Torr. Metals are then deposited at a base pressure of $1 \times 10^{-6}$ Torr. In some cases, sputter deposition is used to deposit, for instance, the NiCu thermocouples used in Chapters 4 and 7 using a Kurt J. Lesker sputter system at a base pressure of $5 \times 10^{-8}$ mbar, a power of 200 W, Ar gas pressure of $3 \times 10^{-3}$ mbar and at a rate of 1.6 nm/sec.
5. **Lift-off and wire-bonding**: Sample is immersed in a warm Acetone (45 °C) for 10-15 minutes resulting in the removal of the resist and metal on top of it. After the completion of the fabrication step, each $2 \times 2 \text{mm}^{-2}$ devices are glued on top of a 16-pin chip carrier and connections between the contact pads on the sample and the chip carrier are made using AlSi wires (Al 99% and Si 1%).

### A.2.1 Note on the fabrication of nanopillar spin valves

The nanopillar spin valve devices in chapters 3, 4 and 5 were fabricated using a cross-linked PMMA as an insulating layer between the top and bottom contacts, which is different from earlier methods that often require dry or wet etching steps to define the nanopillar. In our method, the crucial step involves first defining a contact hole using an EBL step. After the deposition of the nanopillar on a bottom contact, an opening to the top of the nanopillar and an encapsulation layer around it is achieved using a single polymer layer. After defining the opening using an EBL step followed by development step in 1:3 mixture of MIBK:IPA solution, a $1.5 \times 1.5 \mu m^{-2}$ area around the nanopillar is exposed with a dose of 18 mC/cm$^{-2}$ enough to cross-link the exposed region. A lift-off process in hot acetone hence removes the resist from the wafer except the cross-linked PMMA that has the contact hole at the middle that serves as a gap opening for the top contact. Finally the top Au contact is defined. A dip in the Au lead at the center of the device [see Fig. A.1(c)] is the contact hole.

### A.2.2 Note on the fabrication of graphene devices

The graphene devices prepared for the thermoelectric effect studies were prepared using optical and e-beam lithography methods. The graphene deposition on the Si substrate was done by the mechanical ex-foliation (Scotch tape) method. The graphene was mechanically cleaved from a highly order pyrolytic graphite (HOPG) from GE Advanced Cermaics, grade ZYA. Optical and atomic force microscopy were employed for the selection, positional marking, thickness and quality identification. After a suitable graphene flake (2-5 $\mu$m wide and several tens of microns long) has been identified, the thermoelectric graphene device is fabricated in 2-step EBL processing with subsequent deposition of Au electrical contacts (e-beam evaporation) and Ni$_{45}$Cu$_{55}$ thermocouples (sputter deposition).
Appendix B

Measurement technique

All devices investigated in this thesis were measured using standard ac measurement techniques using a lock-in amplifier. A lock-in amplifier is a widely used phase sensitive detection technique that allows for large signal to noise ratios compared to dc measurements. By mixing a signal with its internal reference oscillator and using its low bandwidth, with a very narrow frequency spectrum, it can effectively filter out wide band noise.

The measurement setup, which is fully controlled by National instrument’s computer software LABVIEW, consists of homebuilt IV-measurement box (with a current source and signal amplifier), three digital lock-in amplifiers (SR830) and a GMW 5403 electromagnet with a power supply. The sample, that is wire bonded and mounted on a chip carrier, is connected to a switch box that is used to selectively connect specific contacts and is placed in between the two poles of the electromagnet. In the angle dependent measurements, the chip carrier is mounted on a rotatable sample holder that is controlled by an automated stepper motor.

In a typical measurement, the SR830 lock-in amplifier is used to provide a sinusoidal ac voltage as input to the IV-measurement box that converts it to an ac current. This ac current is sent to the sample and the ac voltage response from sample is fed back to the lock-in amplifier via the IV-measurement box, which can amplify the signal with a of upto $10^4$. Often two or more lock-in amplifiers are used to identify signals that are nonlinear with the excitation current, such as Joule heating and temperature driven changes in electrical and thermal transport effects. In our measurements, usually the voltage response from a sample $V(t)$, for low biasing conditions, is linear in the applied current $I(t)$. However, for large biases or highly nonlinear systems, additional signals that are integer multiples of the excitation frequency (nonlinear signals) are also observed. When an ac current $I = \sqrt{2}I_0 \sin(\omega t + \phi)$, with angular frequency $\omega = 2\pi f$ and phase $\phi$ is applied to a device under test, the voltage response from the sample can be written as

$$V(t) = IR_1 + I^2R_2 + I^3R_3 \cdots .$$

(B.1)

Here $R_n$ is $n^{th}$ order response. A lock-in amplifier, which is tuned to a respective harmonic frequency, can identify these various high order signals. The $n^{th}$ har-
monic output voltage of the lock-in amplifier is given by the integrated value of the multiplication of the measured voltage with a reference signal as

\[ V^{nf} = \frac{\sqrt{2}}{T} \int_{0}^{T} \sin(n\omega s + \phi)V_{in}ds \]  

(B.2)

The first, second and third harmonic r.m.s. voltages measured at the lock-in amplifiers are related to \( R_i \) as

\[ V^{1f} = R_1 I_0 + \frac{3}{2} R_3 I_0^3 \quad \text{with} \quad \phi = 0^\circ \]  

(B.3a)

\[ V^{2f} = \frac{1}{\sqrt{2}} R_2 I_0^2 \quad \text{with} \quad \phi = -90^\circ \quad \text{and} \]  

(B.3b)

\[ V^{3f} = -\frac{1}{2} R_3 I_0^3 \quad \text{with} \quad \phi = 0^\circ \]  

(B.3c)

Equation (B.3a) indicates that, in the large biasing regime, the first harmonic resistance \( R^{1f} = V^{1f}/I_0 \) is not equal to the first order response \( R_1 \). It is therefore important to make correction for the contribution from the third harmonic. When the system under consideration is also highly nonlinear, such as in the case of magnetic tunnel junctions, higher harmonic responses need to be recorded up to the contributions where no clear signal is observed above the noise level.